National Kaohsiung First University of Sci. & Tech.

矽基非等向性濕蝕刻

Silicon Anisotropic Wet Etching

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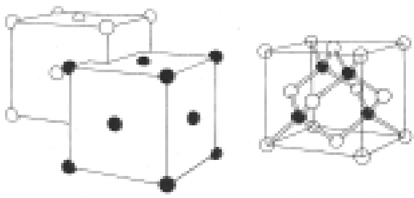
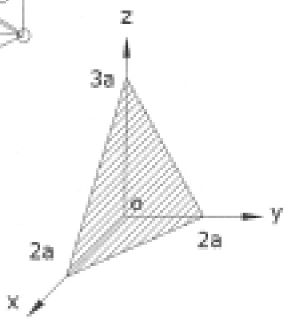
晶格方向

- 矽為鑽石結構：兩個相互交替的面心複晶格



- Miller Indices（密勒指標）
  - 平面法向量
  - 平面截距之倒數
  - 元件電特性、基材蝕刻速率與晶格方向有很大的關係

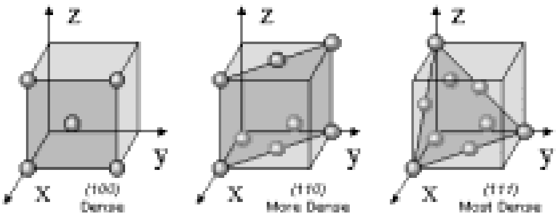


MEMS Lab.

Miller Index

- 若將密勒指標配合不同括號使用，則代表不同的集合
  - (hkl)：小括號代表單一晶面，$(\bar{1}00)$代表與X軸截距為負的平面
  - {hkl} ：代表具相等對稱平面的集合{100}代表以下六平面的集合 $(100),(010),(001),(\bar{1}00),(0\bar{1}0),(00\bar{1})$
  - [hkl]：代表(hkl)平面的法向量，如[100]垂直於(100)平面
  - <hkl>：代表等效方向的集合

Miller indices identify crystal planes from the unit cell



Characteristics of Etching Techniques

- Selectivity
  - Etching method removes a specific material but does not (or only slightly) remove other materials
- Directional Property
  - Isotropic: etching speed is the same in every direction.
  - Anisotropic: etching speed is NOT the same in every direction.

Bulk Micromachining

- Structuring of silicon in three dimensions using anisotropic etching
- High aspect ratio is possible.
- Crystal orientation decides the structure geometry

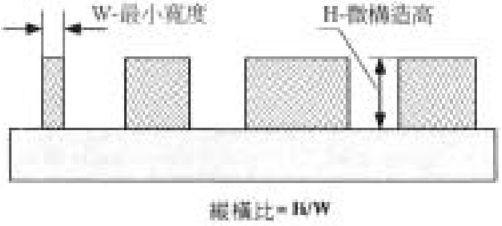


圖 3.6 縱橫比的意義

Etching Mechanisms

- Chemical Wet Etching
  - Dipping the substrate into an etching bath or spraying it with the etching solution.
  - Etching solution is acidic or alkaline to dissolve the material to be removed.
- Dry Etching
  - Expose the substrate to an ionized gas.
  - Chemical or physical interaction occur between the ions in the gas and the atoms of the substrate.

MEMS材料與常用之蝕刻液

- Si (Single-Crystal Silicon, Polysilicon)
  - Anisotropic etching: KOH (Potassium Hydroxide), EDP (Ethylene-Diamine Pyrocatecol), TMAH
  - Isotropic etching: HNA etching system, hydrofluoric (HF), nitric (HNO_3), acetic acid (CH_3COOH)
- SiO_2 (Thermal SiO_2, LTO, PSG)
  - Release process using 49% HF
  - Oxide patterning using buffered HF (28 ml 49% HF, 170 ml H_2O, 113 g NH_4F), also know as Buffered Oxide Etch (BOE)
- Quartz (Crystalline SiO_2): Anisotropic etching in heated HF and ammonium fluoride (NH_4F) solution
- SOG: dissolved in $HCl:HF:H_2O$

Isotropic Etching

- Chemical wet etching for amorphous or polycrystalline (ex. polysilicon) is always isotropic.
- Cavities with rounded off edges (undesired in design).
- Resist is undercut.
- Limited in deep forming.
- Dimension control is difficult.
- Useful in surface micromachining.

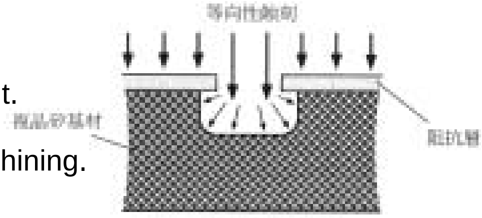


圖 4.6 等向性化學溼蝕刻。

Anisotropic Etching

- Etching speed depends on the crystal’s orientation in single-crystal silicon.
- Typical etching rate : {110}>{100}>>{111}
- Precisely structured in 3D.

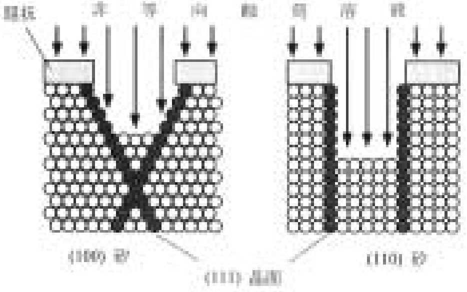


圖 4.5　單晶矽的非等向蝕刻。

矽非等向蝕刻液的種類

- 有機溶液：TMAH、聯氨(Hydrazine)及EDP
  - 聯氨(Hydrazine)及EDP具毒性且不穩定
  - TMAH與IC製程相容，可以二氧化矽作為蝕刻阻擋層(etching mask)，無毒，但蝕刻速率較低
- 鹼液：KOH, NaOH, LiOH, CsOH, NH_4OH,並可添加異丙醇(IPA)等
  - KOH低毒性、較佳的蝕刻面，故常被使用，但鉀離子會污染IC製程
- 影響蝕刻速率除了晶格方向與蝕刻液的種類外，尚包括溫度、濃度、攪拌形式、滲雜種類、表面缺陷、薄膜應力、表面雜質的殘留、氣泡、PH值等

非等向蝕刻液的比較

	TMAH	EDP	KOH
操作及處理	易	難	易
毒性	無	有	無
矽的蝕刻速率	～1 μm/min	0.02-1 μm/min	1-2 μm/min
蝕刻面平坦度	多變*	極佳	佳
IC 製程相容性	相容	相容	不相容
硼蝕刻停止	$>10^{20}/cm^3$	$\geqq 5 \times 10^{19}/cm^3$	$>10^{20}/cm^3$
其他材料的選擇性	Al**	Ta, Au, Cr, Ag, Cu	N/A
蝕刻阻擋層	Si_3N_4, SiO_2	Si_3N_4, SiO_2	Si_3N_4

Note: etch rate of SiO_2=435 nm/hr at 80°C 30% KOH

溼蝕刻的機制

- 濕蝕刻的機制
  - 蝕刻液由邊界層外傳輸至蝕刻表面
  - 蝕刻液與蝕刻面反應產生生成物
  - 生成物由蝕刻表面傳輸至邊界層外

$$Si + 2OH^- \rightarrow Si(OH)_2^{++} + 4e^-$$

$$4H_2O + 4e^- \rightarrow 4OH^- + 2H_2$$

$$Si(OH)_2^{++} + 4OH^- \rightarrow SiO_2(OH)_2^{--} + 2H_2O$$

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{--} + 2H_2$$

- 外加攪拌可產生強制對流，增加第一、三道的值量傳遞過程，而第二道過程為化學反應
  - 溫度越高蝕刻速率越高，但蝕刻面粗糙度將變差
  - 固定溫度下存在一蝕刻速率最高的蝕刻液濃度

Silicon Lattice Structure

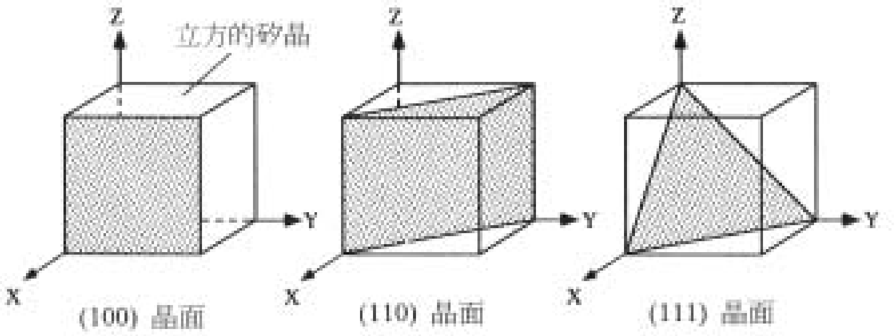
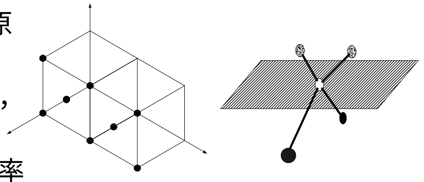


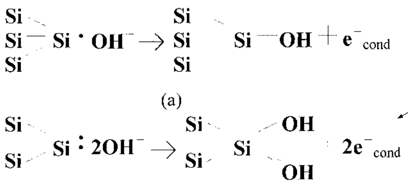
圖 4.7　矽晶格構造之晶面。

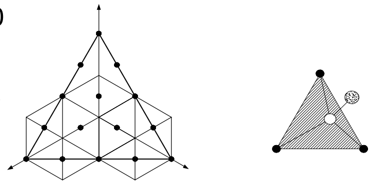
晶格鍵結與蝕刻

- {100}與{111}面的共價鍵與懸垂鍵
  - KOH蝕刻時蝕刻液的OH⁻與矽原子的懸垂鍵反應
  - {111}有三個共價鍵，強度較高，故蝕刻速率低
  - {100}只有兩個共價鍵，蝕刻速率高
  - 速率R{111}/R{100} = 1:80~1:120



Si atoms on a {100} plane

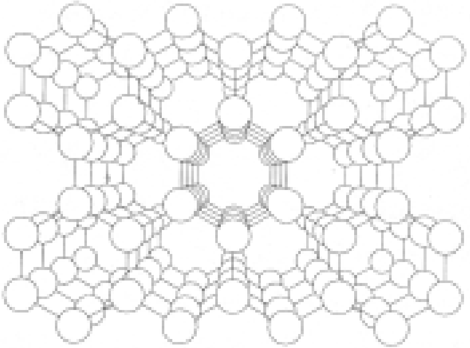




Si atoms on a {111} plane

單晶矽的晶格方向與蝕刻速率

- {110}晶面雖然有三個共價鍵，但因晶面的原子排列鬆散，以致蝕刻液對矽原子結構產生穿遂效應(Channeling effect)，造成蝕刻速率較快(Hesketh, 1993)。



Bulk Micromachining

- 蝕刻幾何形狀將沿著(111)晶面被切割
- 常用於橋、樑、薄膜等特徵的構造

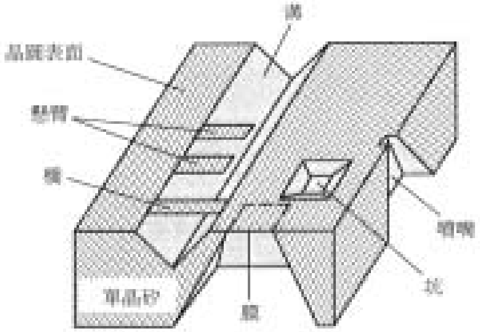


圖 4.14　各種立體微機械加工構造，根據 [Howe 90]。

Basic Structures in Silicon

- Anisotropic Etching of Silicon

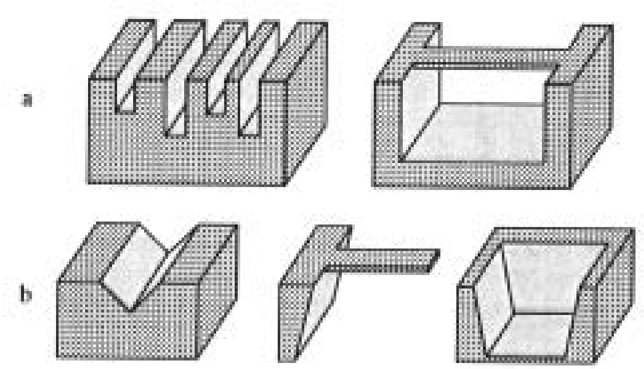


圖 4.9 能夠在 a (110) 矽；b) (100) 矽上製成之基本構造。

晶格面與角度關係

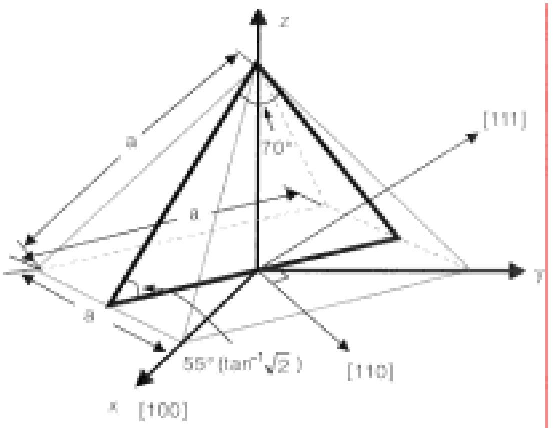
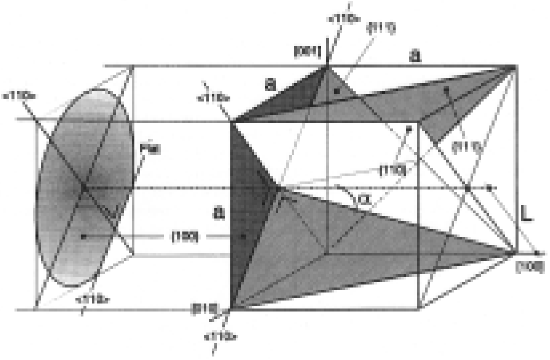


圖 3.10 不同矽晶格面間之幾何及角度關係。

晶圓方向

- {100}晶圓的蝕刻夾角
  - {111}與{110}方向的夾角 $\alpha = \tan^{-1}((\sqrt{2}/2)/1) = 35.26°$
  - 亦可利用<111>與<110>向量的餘弦定理求出兩向量的夾角

$$1\cdot1+1\cdot1+1\cdot0=\sqrt{1+1+1}\sqrt{1+1+0}\cos\alpha$$



{100}晶圓的晶面安排與蝕刻停止面

- {100}晶圓的主切邊為<110>方向

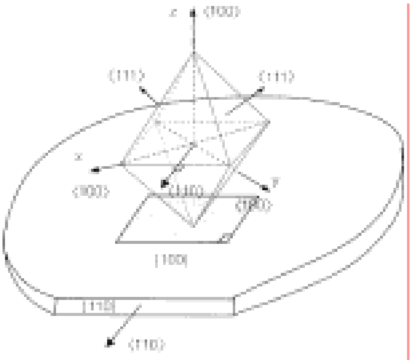
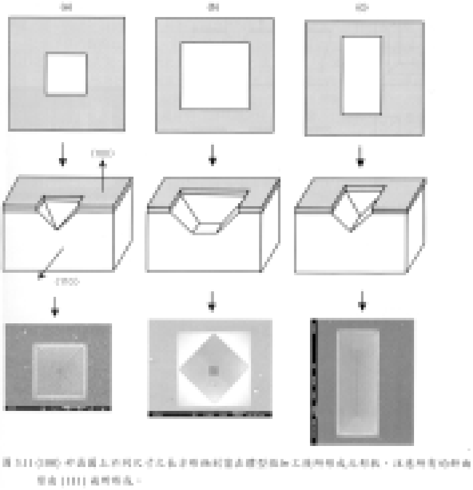


圖 3.9 (100) 矽晶圓之晶圓平面及大平邊與矽晶格各平面間之關係。

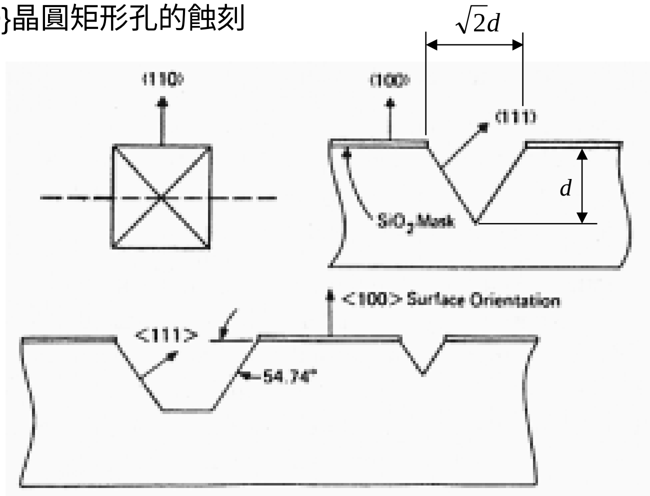
{100}晶圓上各種矩形的蝕刻形狀

- 最終蝕刻面由{111}面所定義



{100}晶圓的蝕刻角度

- {100}晶圓矩形孔的蝕刻



{100}晶圓的蝕刻夾角

- <111>與<100>向量的餘弦定理

$$1\cdot1+1\cdot0+1\cdot0=\sqrt{1+1+1}\sqrt{1+0+0}\cos\theta,\ \theta=54.74$$

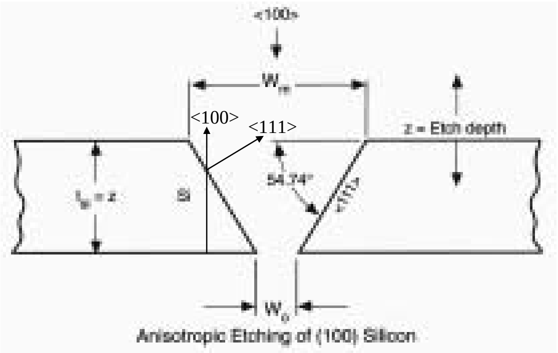
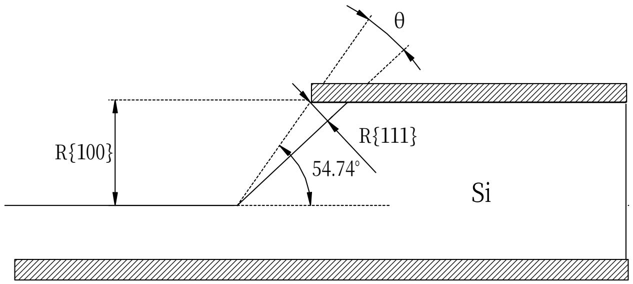


Figure 4.8 Relation of bottom cavity plane width with mask opening width.

Undercut of {100} Wafer

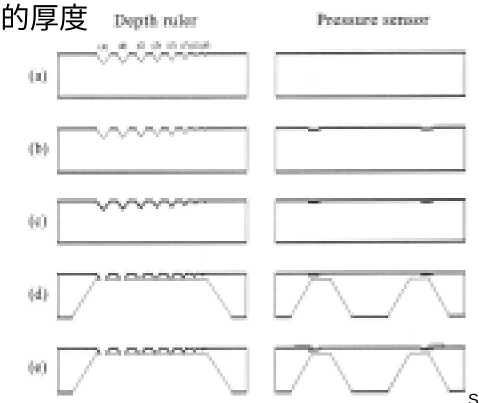
- Undercut due to finite selectivity between the etch rates of {111} and {100}.

$$\tan\theta=\sqrt{1/3}\times R\{111\}/R\{100\}$$



{100} V-Groove Depth Ruler

- 利用{100}晶圓V槽寬深比為$\sqrt{2}:1$ 的特性，由被蝕穿的孔判斷剩餘薄膜的厚度



Source: 認識微機電—楊龍杰

圖 3-13 配合壓力計製作之 V 型槽深度尺製程，左列是深度尺，右列是壓力計：(a) 深度尺蝕刻；(b)壓電阻佈植；(c)長氮化層；(d)背面蝕刻；(e)長鋁金屬線 [5]

Anisotropic Etching in {110} Wafer

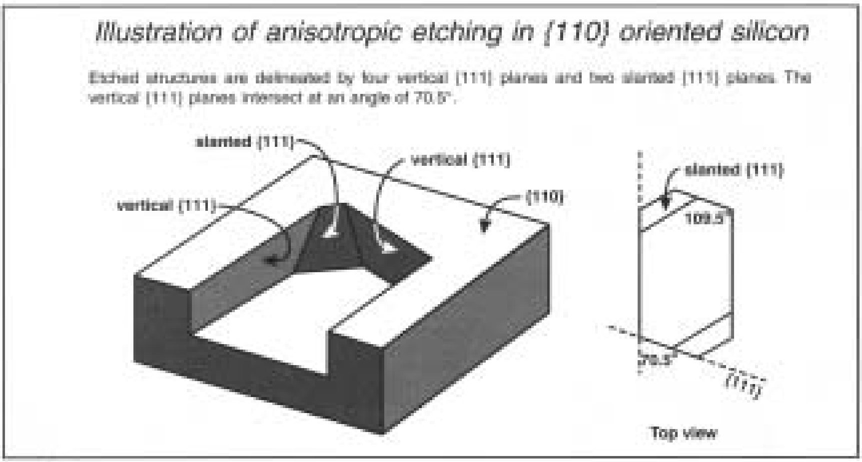


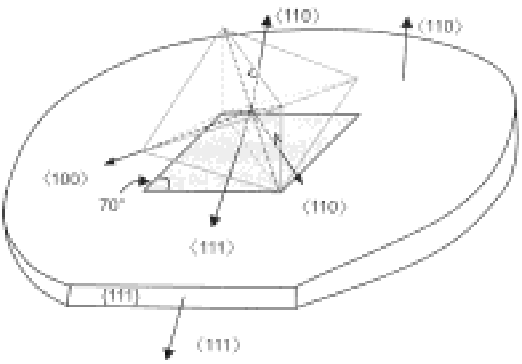
Illustration of anisotropic etching in {110} oriented silicon

Etched structures are delineated by four vertical {111} planes and two slanted {111} planes. The vertical {111} planes intersect at an angle of 70.5°.

Inset 4.4

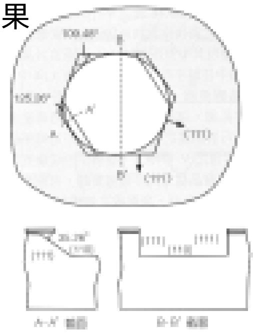
{110}晶圓的晶面安排與蝕刻停止面

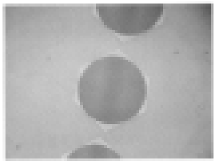
- {110}晶圓的主切邊為{111}面

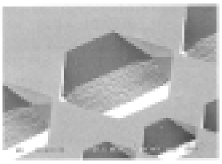


{110}晶圓的蝕刻

- 原形開孔的蝕刻結果

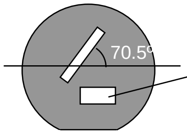


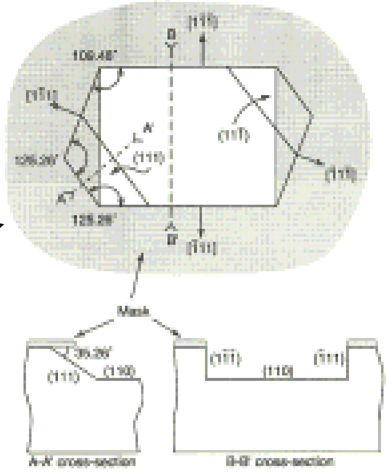

(110)-[illegible]


(110) [illegible]

Mask Patterning and Etching in {110} Wafer

- 在{110}晶圓以非等向性蝕刻長深槽，其長邊 [111]平行於主切邊，或與主切邊有70.5 ° 的夾角時，可獲得垂直的蝕刻牆邊

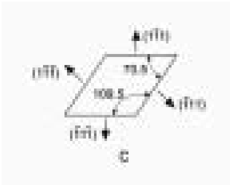


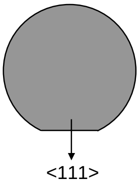


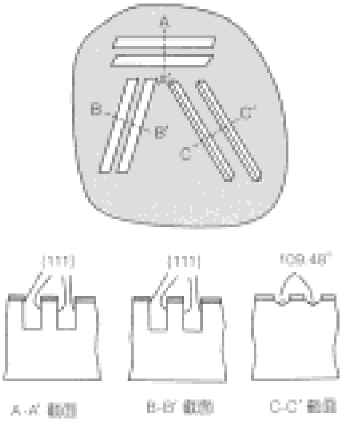
- {110}晶圓所蝕刻的深槽的兩端則由另外兩個[111]面所定義，而呈現多稜面的幾何形狀

Anisotropic Etching in {110} Wafer

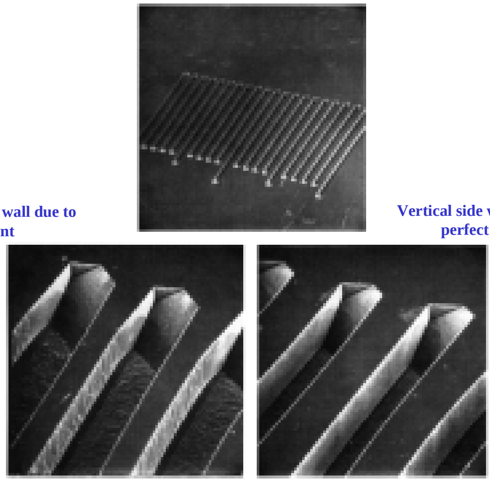
- {110}晶圓上不同角度矩形槽與蝕刻斷面的關係







Long Narrow Grooves in a <110> Wafer



Rough side wall due to misalignment

Vertical side wall due to perfect alignment

Figure 4.33 Long, narrow grooves in a <110> wafer. These U-grooves are used as test patterns. Test pattern of U-grooves in a <110> wafer help in the alignment of the mask. Final alignment is done with the groove that exhibits the most perfect long perpendicular walls.

Selection of Silicon Wafer

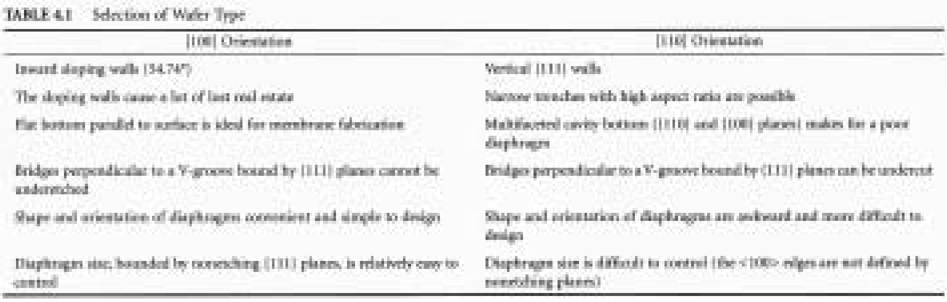
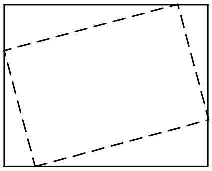


TABLE 4.1 Selection of Wafer Type

{100} Orientation	{110} Orientation
Inward sloping walls (54.74°)	Vertical {111} walls
The sloping walls cause a lot of lost real estate	Narrow trenches with high aspect ratio are possible
Flat bottom parallel to surface is ideal for membrane fabrication	Multifaceted cavity bottom ({110} and {100} planes) makes for a poor diaphragm
Bridges perpendicular to a V-groove bound by {111} planes cannot be underetched	Bridges perpendicular to a V-groove bound by {111} planes can be undercut
Shape and orientation of diaphragms convenient and simple to design	Shape and orientation of diaphragms are awkward and more difficult to design
Diaphragm size, bounded by nonetching {111} planes, is relatively easy to control	Diaphragm size is difficult to control (the <100> edges are not defined by nonetching planes)

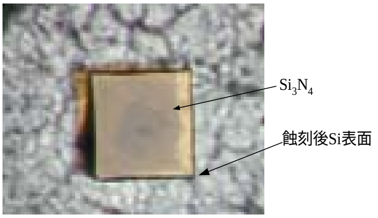
矽結構立體微細加工

- 凸角矽微結構蝕刻缺陷
  - 底部蝕刻（underetch）
  - 底切（undercut）



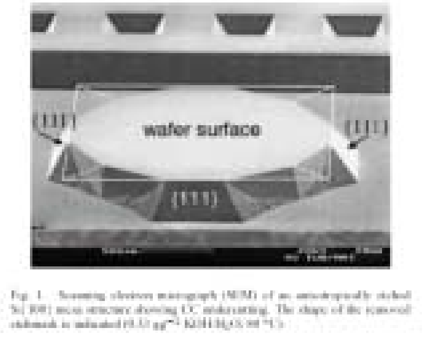
- - - -對位不準

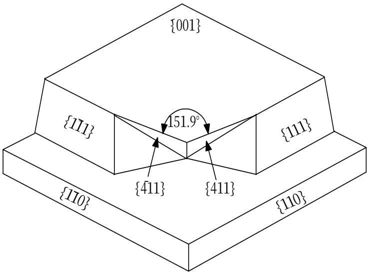
———實際蝕刻



矽結構凸角底切的現象

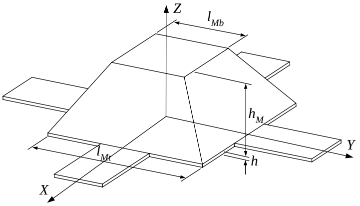
- 裸露的矽凸角特徵，在KOH蝕刻時產生底切的現象

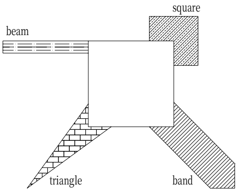


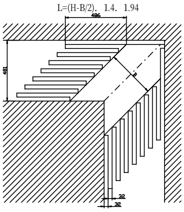


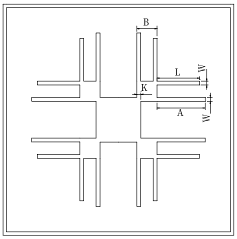
化學濕蝕刻的凸角補償

- 角落補償圖形設計原理
  - <100>延伸法
  - <110>延伸法
  - 狹窄空間的光罩角落補償圖形



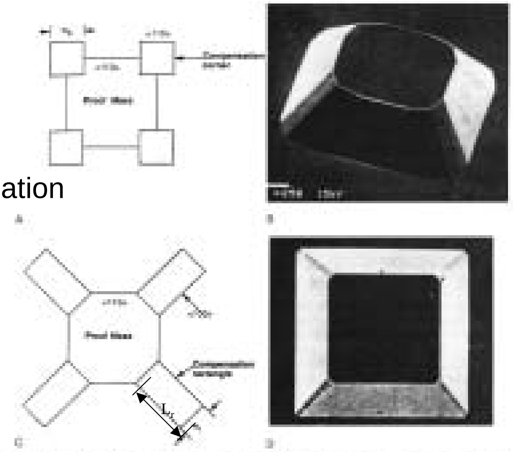




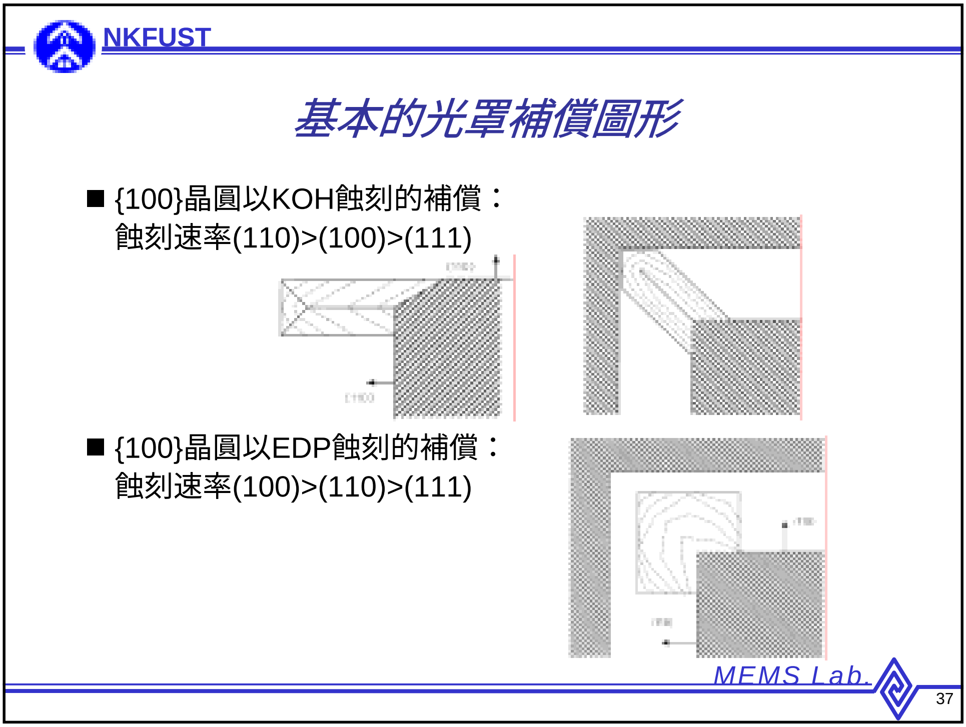


基本角落補償

- Square Compensation
  - W_s=etching depth
- <100> Band Compensation
  - W_r=2(etching depth)
  - L_r=1.6W_r



[illegible]



NKFUST

基本的光罩補償圖形

- {100}晶圓以KOH蝕刻的補償：
  蝕刻速率(110)>(100)>(111)
- {100}晶圓以EDP蝕刻的補償：
  蝕刻速率(100)>(110)>(111)

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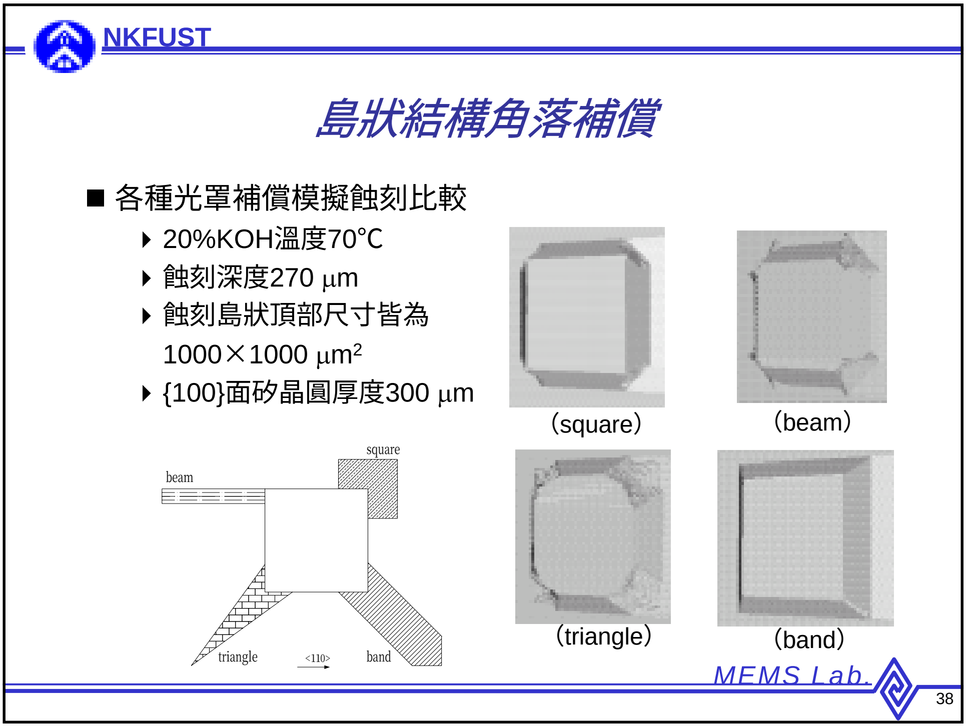

NKFUST

島狀結構角落補償

- 各種光罩補償模擬蝕刻比較
  - 20%KOH溫度70℃
  - 蝕刻深度270 μm
  - 蝕刻島狀頂部尺寸皆為 1000×1000 μm²
  - {100}面矽晶圓厚度300 μm

(square)

(beam)

(triangle)

(band)

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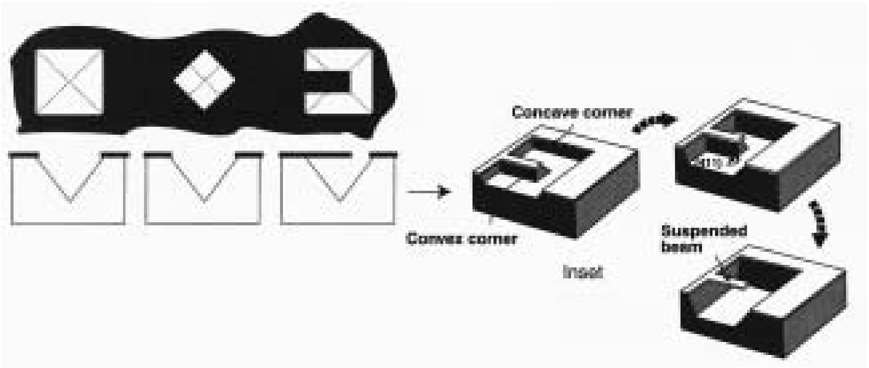
以濕蝕刻製作懸樑



蝕刻底切所造成的特徵

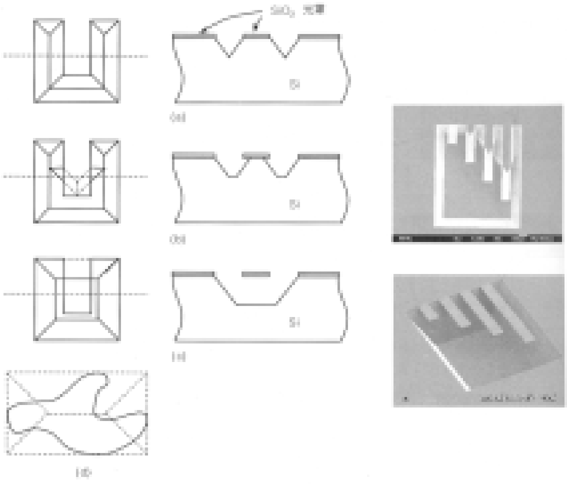


圖 3.12 [illegible]

滲雜(Doping)的方式

- Diffusion
  - Furnace heating.
  - The doping atoms from the surrounding gas or a thin preapplied surface layer.
  - Main difficulty
    - Determination of the absolute concentration of the doping.
    - Only create a doping profile on the surface of a wafer.
- Ion implantation
  - Shooting charged doping ions, which are externally accelerated in a vacuum, into the silicon wafer.
  - The ions can penetrate up to a few micrometers below the surface.
  - The doping concentration gets an improved homogeneity, and the doping profile under the wafer's surface can be controlled more exactly.

Comparison of Two Doping Methods

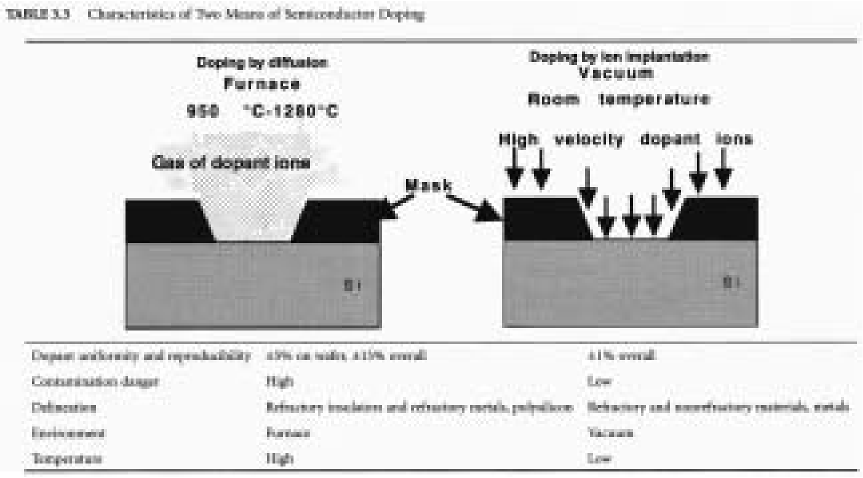


TABLE 3.3 Characteristics of Two Means of Semiconductor Doping

	Doping by diffusion	Doping by ion implantation
Dopant uniformity and reproducibility	±5% on wafer, ±15% overall	±1% overall
Contamination danger	High	Low
Delineation	Refractory insulators and refractory metals, polysilicon	Refractory and nonrefractory materials, metals
Environment	Furnace	Vacuum
Temperature	High	Low

Source: Fundamentals of Microfabrication, Madou

P+ Etch-Stop

- Doping the silicon substrate with germanium, phosphorus or boron atoms
- P^+ (Boron) concentration of about 10^{20} cm^{-3} or higher will drastically reduce etching rate
- Doping
  - Diffusion method
    - Difficult to get a uniform membrane thickness
  - Ion implantation
    - Good concentration and depth control but slow
    - 2 μm with a concentration of 10^{20} cm^{-3}, a 150 μA implanter needs up to an hour per wafer

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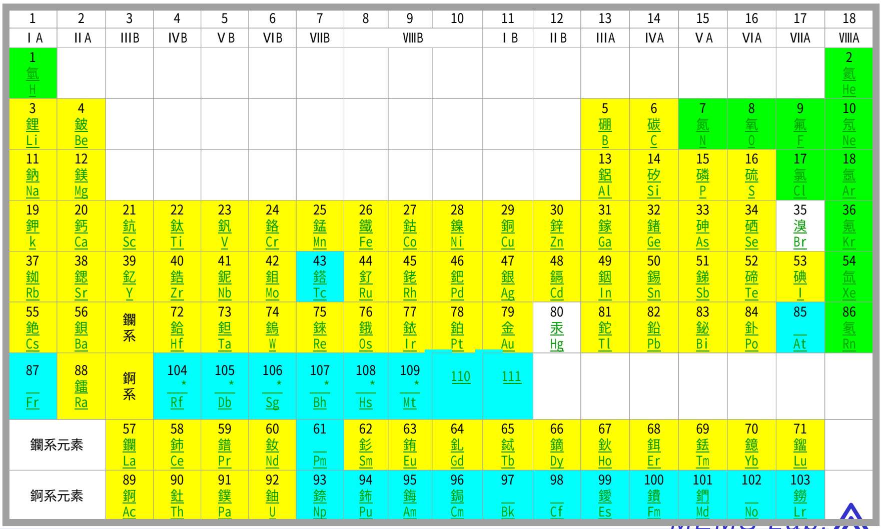
化學週期表



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
I A	II A	IIIB	IVB	V B	VI B	VIIB	VIIIB			I B	II B	IIIA	IVA	V A	VIA	VIIA	VIIIA
1 氫 H																	2 氦 He
3 鋰 Li	4 鈹 Be											5 硼 B	6 碳 C	7 氮 N	8 氧 O	9 氟 F	10 氖 Ne
11 鈉 Na	12 鎂 Mg											13 鋁 Al	14 矽 Si	15 磷 P	16 硫 S	17 氯 Cl	18 氬 Ar
19 鉀 k	20 鈣 Ca	21 鈧 Sc	22 鈦 Ti	23 釩 V	24 鉻 Cr	25 錳 Mn	26 鐵 Fe	27 鈷 Co	28 鎳 Ni	29 銅 Cu	30 鋅 Zn	31 鎵 Ga	32 鍺 Ge	33 砷 As	34 硒 Se	35 溴 Br	36 氪 Kr
37 銣 Rb	38 鍶 Sr	39 釔 Y	40 鋯 Zr	41 鈮 Nb	42 鉬 Mo	43 鎝 Tc	44 釕 Ru	45 銠 Rh	46 鈀 Pd	47 銀 Ag	48 鎘 Cd	49 銦 In	50 錫 Sn	51 銻 Sb	52 碲 Te	53 碘 I	54 氙 Xe
55 銫 Cs	56 鋇 Ba	鑭系	72 鉿 Hf	73 鉭 Ta	74 鎢 W	75 錸 Re	76 鋨 Os	77 銥 Ir	78 鉑 Pt	79 金 Au	80 汞 Hg	81 鉈 Tl	82 鉛 Pb	83 鉍 Bi	84 釙 Po	85 At	86 氡 Rn
87 Fr	88 鐳 Ra	錒系	104 * Rf	105 * Db	106 * Sg	107 * Bh	108 * Hs	109 * Mt	110	111							
鑭系元素		57 鑭 La	58 鈰 Ce	59 鐠 Pr	60 釹 Nd	61 Pm	62 釤 Sm	63 銪 Eu	64 釓 Gd	65 鋱 Tb	66 鏑 Dy	67 鈥 Ho	68 鉺 Er	69 銩 Tm	70 鐿 Yb	71 鎦 Lu	
錒系元素		89 錒 Ac	90 釷 Th	91 鏷 Pa	92 鈾 U	93 錼 Np	94 鈽 Pu	95 鋂 Am	96 鋦 Cm	97 Bk	98 Cf	99 鑀 Es	100 鐨 Fm	101 鍆 Md	102 No	103 鐒 Lr	

Membrane using P+ Etch-Stop

- Boron doping
- Silicon layer by epitaxy
- Both sides oxidized
- Lithography of the silicon dioxide
- Anisotropic etching

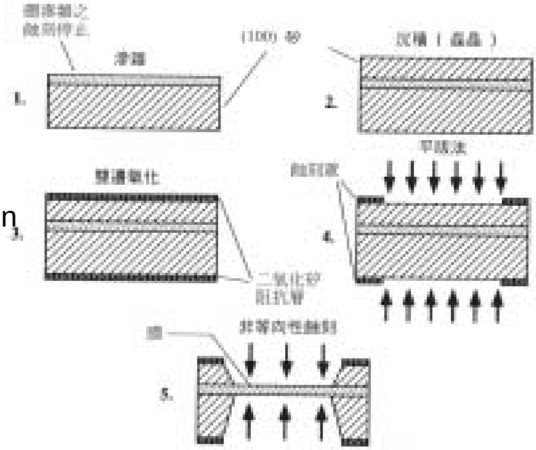


圖 4.15 使用 p⁺ 蝕刻停止技術之膜的生產

Electrochemical Etch-Stop Technique

- Etching process is interrupted when an electric voltage is applied to an np or pn silicon substrate

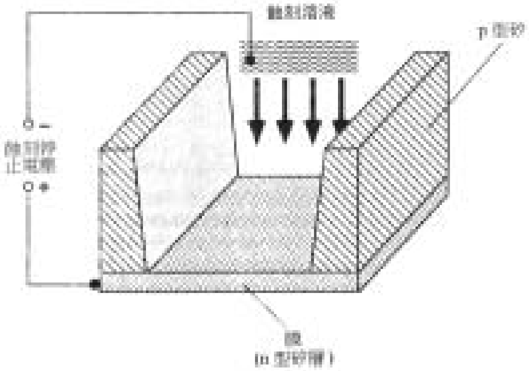
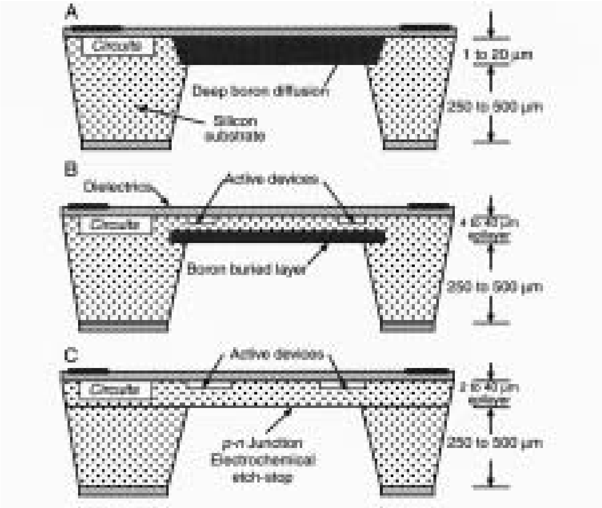


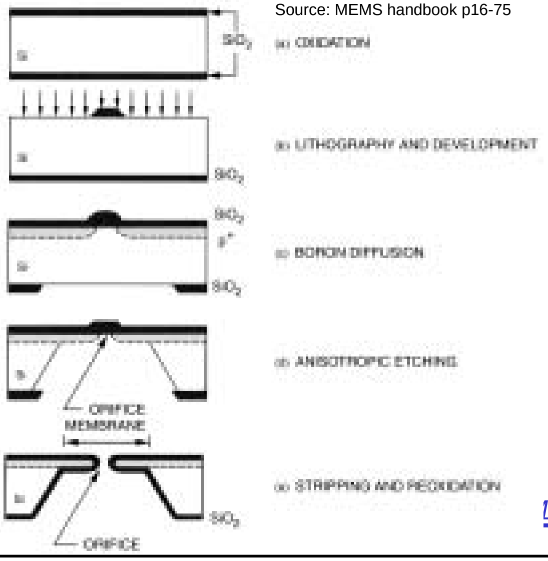
圖 4.16 由電化學的蝕刻停止法生成膜。

以蝕刻停止層製作薄膜結構

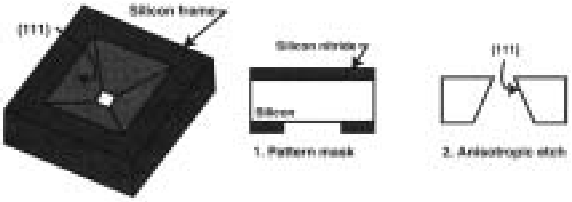


以蝕刻停止層製作薄膜噴嘴

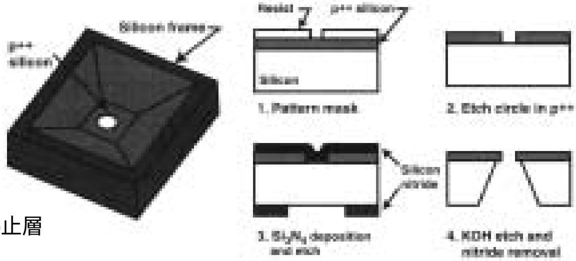
Source: MEMS handbook p16-75



製作Membrane Nozzle的方式的比較



氮化矽方式

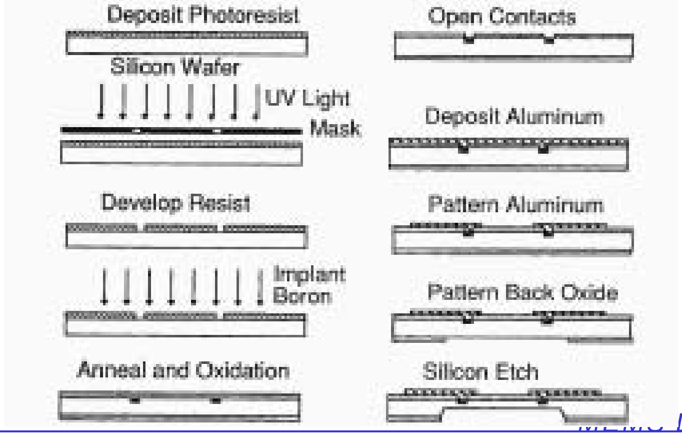


以硼植蝕刻停止層

Piezoresistive Pressure Sensor

- Process steps of piezoresistive sensor using bulk micromachining

Source: Fundamentals of Microfabrication, Madou, Fig 4.1



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- 微機電系統，陳炳輝，五南，（2001）- 第二章