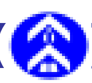

微機電系統相關材料與製作

Materials for Micro-Electromechanical Systems

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Micro-Electro-Mechanical System Lab.

Materials for MEMS

- Ranges of materials
  - Single crystal silicon, Polysilicon, Silicon Dioxide, Silicon Nitride, Metal. Silicon Carbide, Germanium-based materials, Piezoelectric materials, Diamond, III-V Materials.
- Fabrication Methods
  - Crystallization
  - Oxidation
  - Film Deposition
    - Physical Vapor Deposition (PVD)
    - Chemical Vapor Deposition (CVD)
    - Liquid Phase Deposition

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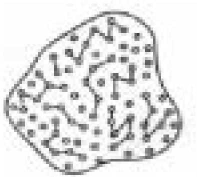
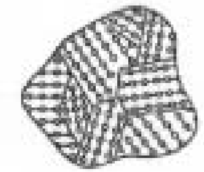
Silicon Crystal Orientation

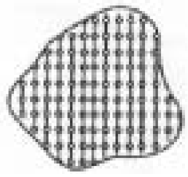
- Crystal Structure
  - Amorphous（非晶體）: No recognizable lump range order
  - Polycrystalline（多晶體）: Completely ordered in grains
  - Crystalline（晶體）: Entire solid is made up of atoms in an orderly array



(a) Amorphous



(b) Polycrystalline



(c) Crystalline

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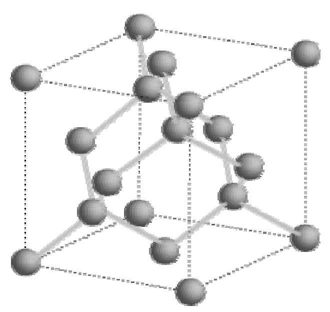
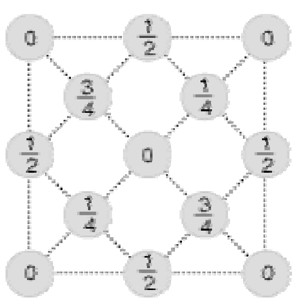
晶體結構

- 鑽石結構或閃鋅晶體結構立方面上的投影





Source:http://hyperphysics.phy-astr.gsu.edu/hbase/solids/sili2.html

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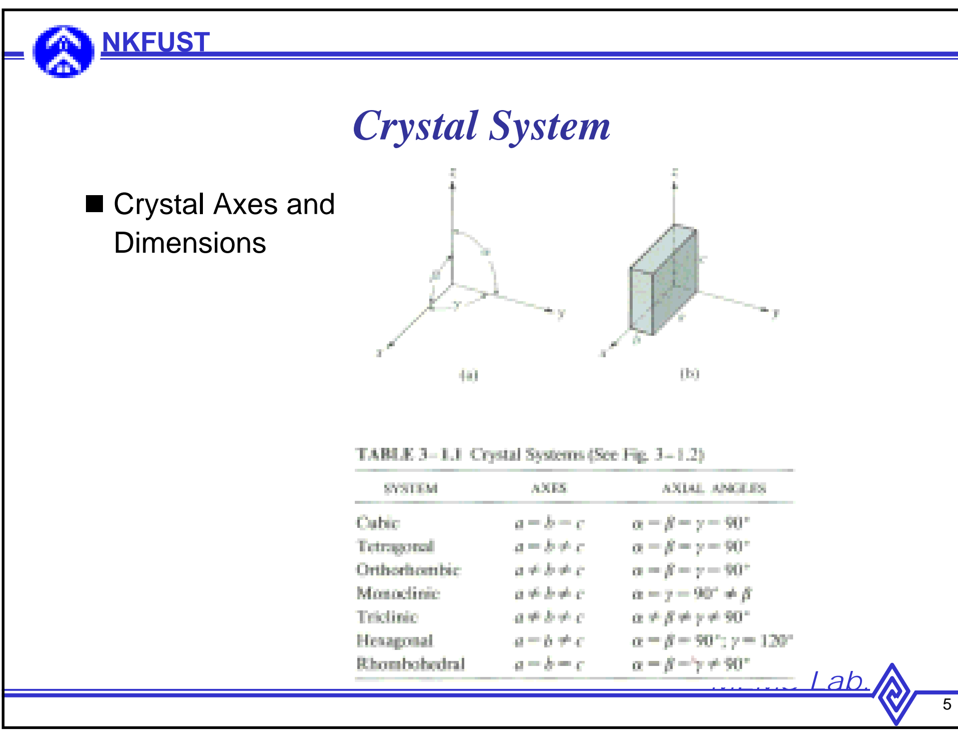
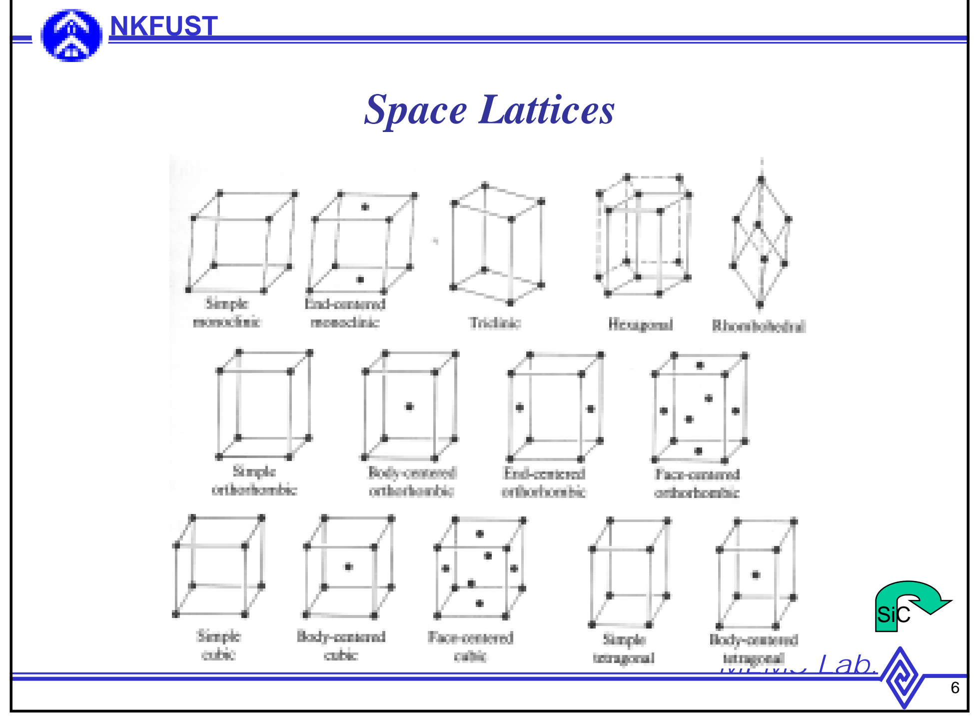


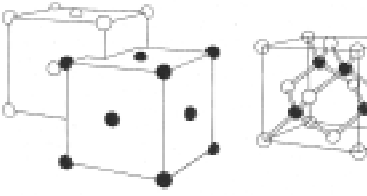
TABLE 3-1.1 Crystal Systems (See Fig. 3-1.2)

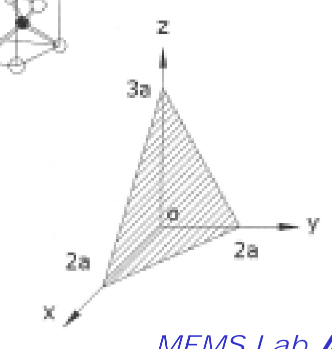
SYSTEM	AXES	AXIAL ANGLES
Cubic	$a = b = c$	$\alpha = \beta = \gamma = 90°$
Tetragonal	$a = b \neq c$	$\alpha = \beta = \gamma = 90°$
Orthorhombic	$a \neq b \neq c$	$\alpha = \beta = \gamma = 90°$
Monoclinic	$a \neq b \neq c$	$\alpha = \gamma = 90° \neq \beta$
Triclinic	$a \neq b \neq c$	$\alpha \neq \beta \neq \gamma \neq 90°$
Hexagonal	$a = b \neq c$	$\alpha = \beta = 90°; \gamma = 120°$
Rhombohedral	$a = b = c$	$\alpha = \beta = \gamma \neq 90°$



晶格方向

- 鑽石結構：兩個相互交替的面心複晶格





- Miller Indices（密勒指標）
  - 平面法向量
  - 平面截距之倒數
  - 元件電特性、基材蝕刻速率與晶格方向有很大的關係

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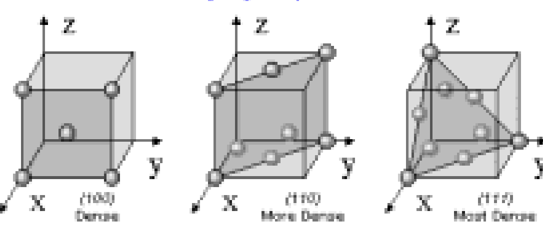
Miller Index

- 若將密勒指標配合不同括號使用，則代表不同的集合
  - (hkl)：小括號代表單一晶面，$(\bar{1}00)$代表與X軸截距為負的平面
  - {hkl} ：代表具相等對稱平面的集合{100}代表以下六平面的集合 $(100),(010),(001),(\bar{1}00),(0\bar{1}0),(00\bar{1})$
  - [hkl]：代表(hkl)平面的法向量，如[100]垂直於(100)平面
  - <hkl>：代表等效方向的集合

Miller indices identify crystal planes from the unit cell



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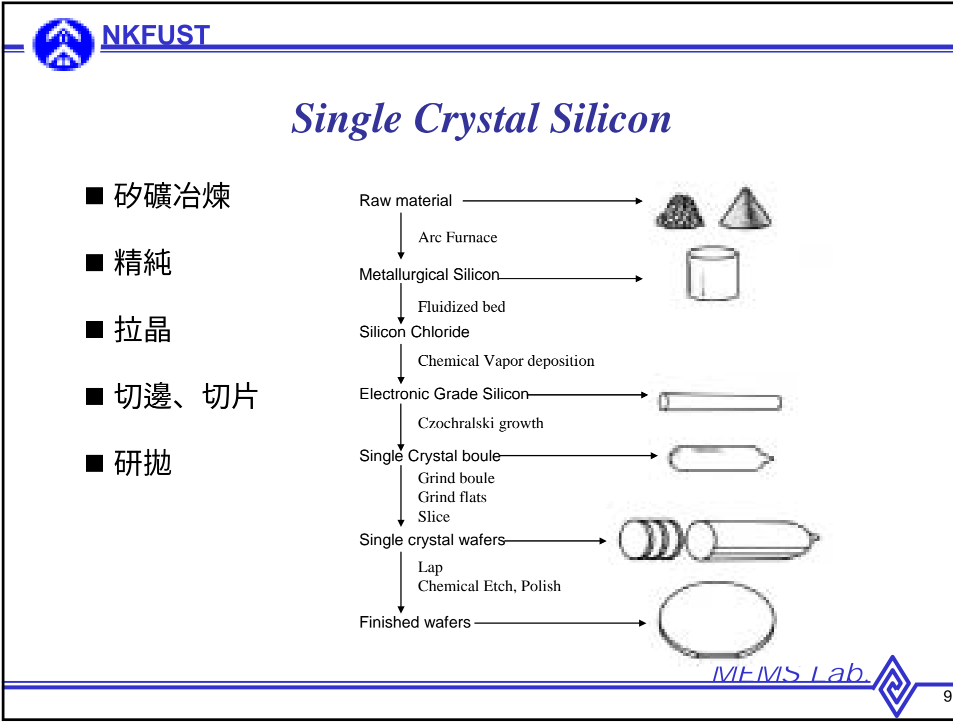

高純度矽的提煉方法

- $SiHCl_3$的H_2還原法
  - Si（固）+3HCl（氣）(220~300°C) →$SiHCl_3$（氣）+H_2（氣）
  - $SiHCl_3$（氣）+H_2（氣）(900~1000°C) →Si（固）+3HCl（氣）
- $SiCl_4$的Zn還原法
  - $SiCl_4$（氣）+2Zn（氣）(950~1000°C) →Si（固）+$2ZnCl_2$（氣）
- $SiCl_4$的H_2還原法（較Zn還原法易於提煉與控制）
  - $SiCl_4$（氣）+$2H_2$（氣）(1100~1200°C) →Si（固）+4HCl（氣）
- SiH_4的熱分解
  - $SiCl_4$ + $LiAlH_4$→SiH_4 + LiCl + $AlCl_3$
  - SiH_4（氣）(1000°C) →Si（固）+$2H_2$（氣）

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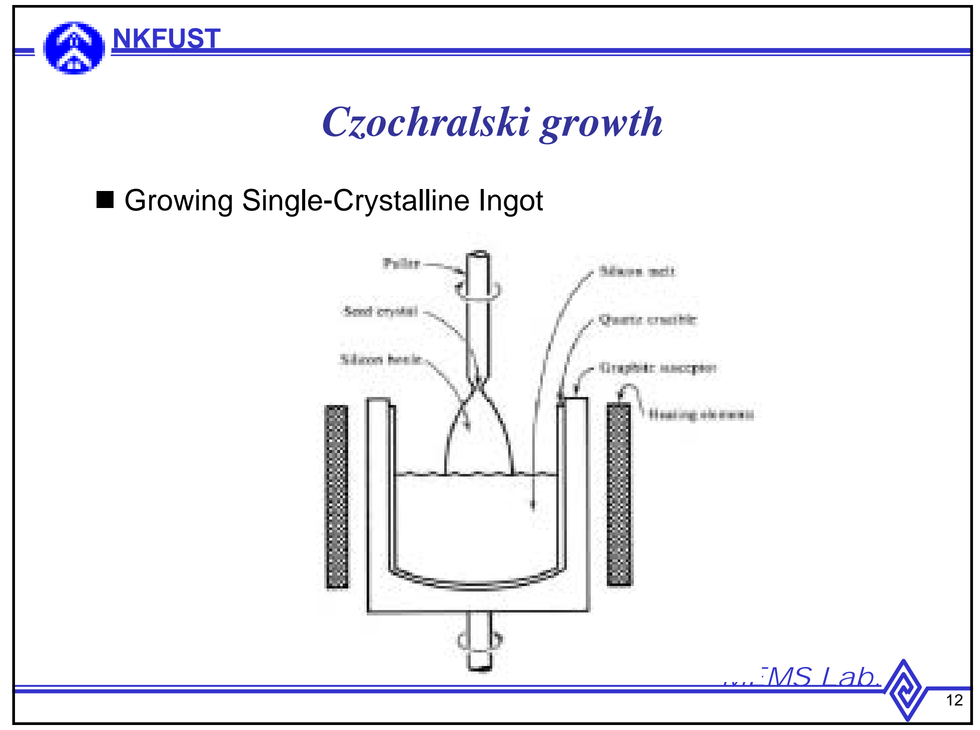
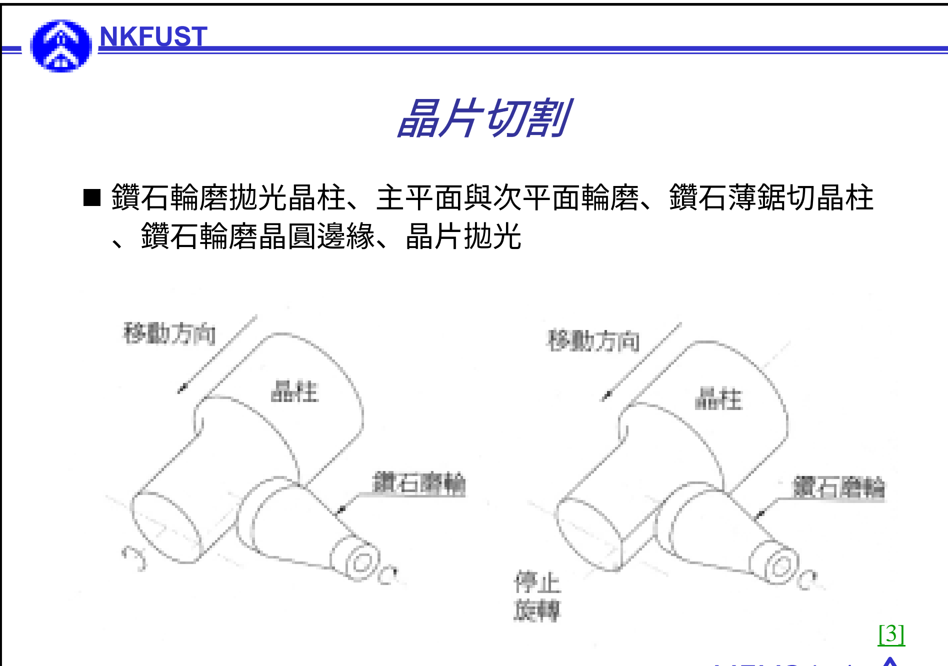
矽的主要物理性質

原子序	14	密度	2.33 克／毫升
原子量	28.09	比熱	0.181 卡／克・℃
單位體積原子數	5×10^{22}	熔化熱	9450 卡／克分子
顏色	銀白色	氣化熱	44086 卡／克分子（25℃）
晶體結構	金鋼石晶格	熱導率	0.20 卡／秒・厘米・℃（25℃）
硬度	莫氏硬度 6.25	延展性	脆
折射率	3.87	電容率	12
熔點	1412℃	沸點	2600℃





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晶圓尺寸規格

參數	100 mm	125 mm	150 mm	200 mm	300 mm
直徑（mm）	100 ± 1	125 ± 1	150 ± 1	200 ± 1	300 ± 1
厚度（mm）	0.5～0.55	0.6～0.65	0.65～0.7	0.7～0.75	0.75～0.8
主要平面長度（mm）	30～35	40～45	55～60	無	無
次要平面長度（mm）	16～20	25～30	35～40	無	無
重量（g）	9.6	17.9	27.8	53	128
表面積(cm^2)	78.5	122.7	176.7	314	707

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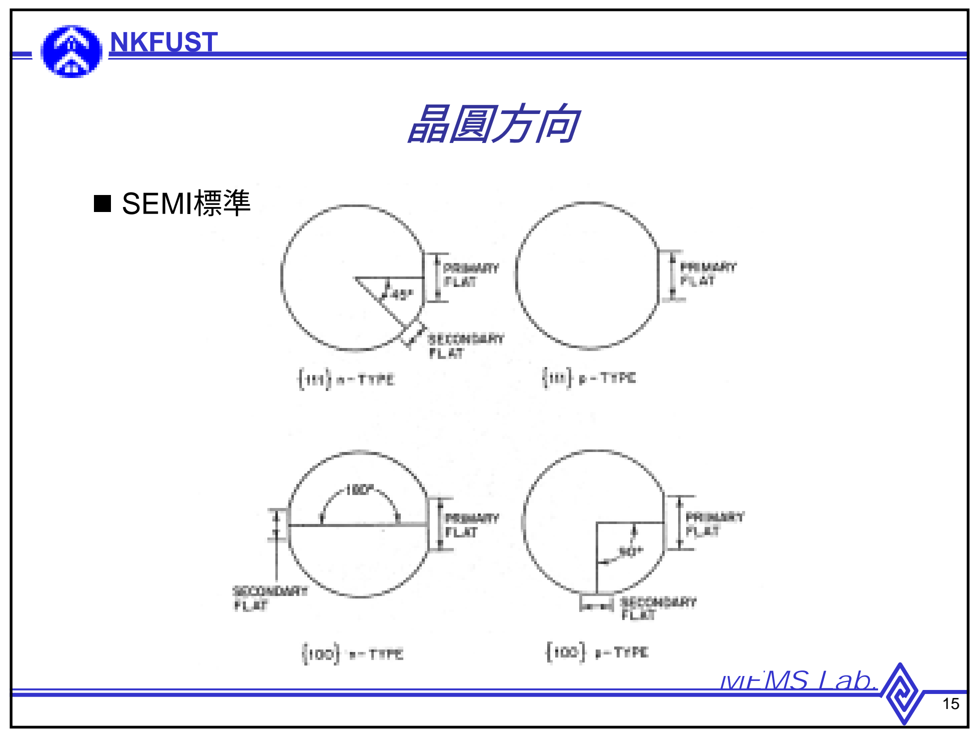
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晶圓方向
SEMI標準
PRIMARY FLAT
45°
SECONDARY FLAT
{111} n-TYPE
PRIMARY FLAT
{111} p-TYPE
180°
PRIMARY FLAT
SECONDARY FLAT
{100} n-TYPE
PRIMARY FLAT
90°
SECONDARY FLAT
{100} p-TYPE
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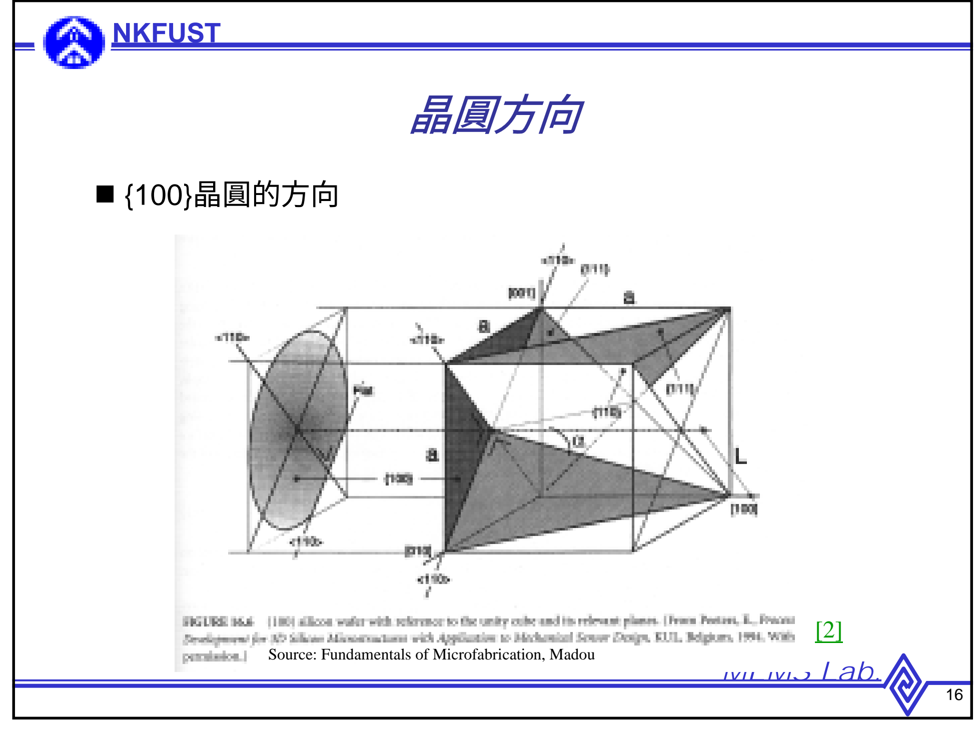
NKFUST
晶圓方向
{100}晶圓的方向
<110>
[001]
a
<110>
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Flat
a
[100]
L
[100]
<110>
[010]
<110>
[2]
Source: Fundamentals of Microfabrication, Madou
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Semiconductor

- Semiconductor: Si（矽）, Ge（鍺）,GaAs（砷化鎵）,InP（銦化磷）,ZnSe（鋅化硒）
- Insulator: SiO_2(二氧化矽）, Si_3N_4 （氮化矽）
- p-type 矽晶片：摻雜硼(B)或第III族元素（Al, In, 等），使半導體產生一個電洞，而成為受體(Acceptor)
- n-type 矽晶片：摻雜砷(As)、磷(P)或第V族元素如銻(Sb) 等，使半導體產生多一個電子的雜質，而成為施體(Donor)

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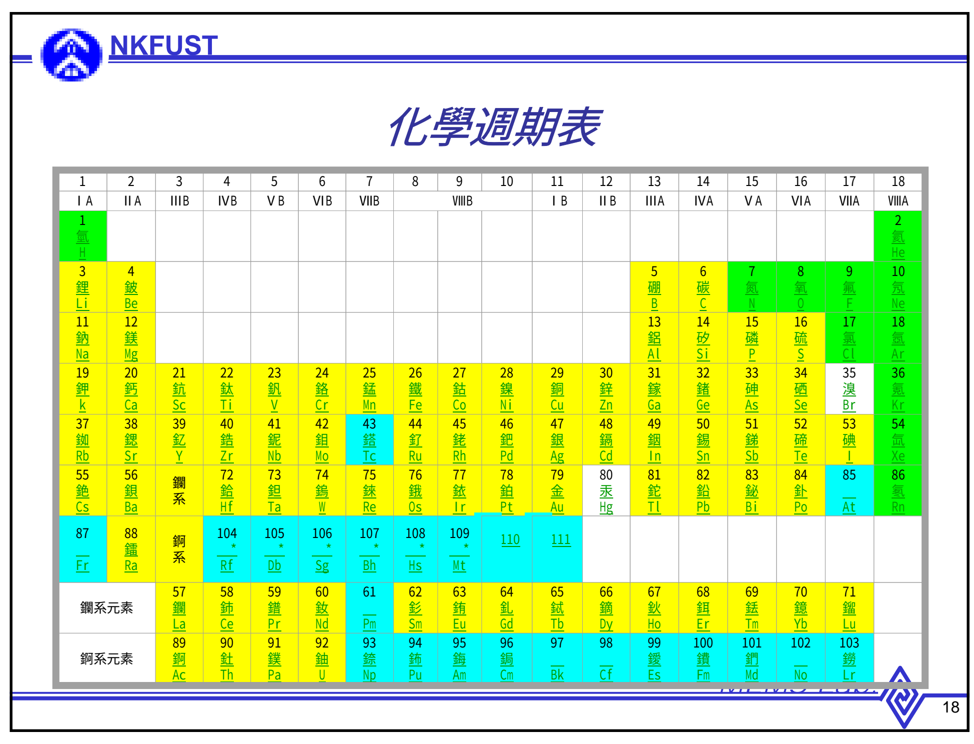

化學週期表

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
I A	II A	IIIB	IVB	V B	VIB	VIIB	VIIIB			I B	II B	IIIA	IVA	V A	VIA	VIIA	VIIIA
1 氫 H																	2 氦 He
3 鋰 Li	4 鈹 Be											5 硼 B	6 碳 C	7 氮 N	8 氧 O	9 氟 F	10 氖 Ne
11 鈉 Na	12 鎂 Mg											13 鋁 Al	14 矽 Si	15 磷 P	16 硫 S	17 氯 Cl	18 氬 Ar
19 鉀 k	20 鈣 Ca	21 鈧 Sc	22 鈦 Ti	23 釩 V	24 鉻 Cr	25 錳 Mn	26 鐵 Fe	27 鈷 Co	28 鎳 Ni	29 銅 Cu	30 鋅 Zn	31 鎵 Ga	32 鍺 Ge	33 砷 As	34 硒 Se	35 溴 Br	36 氪 Kr
37 銣 Rb	38 鍶 Sr	39 釔 Y	40 鋯 Zr	41 鈮 Nb	42 鉬 Mo	43 鎝 Tc	44 釕 Ru	45 銠 Rh	46 鈀 Pd	47 銀 Ag	48 鎘 Cd	49 銦 In	50 錫 Sn	51 銻 Sb	52 碲 Te	53 碘 I	54 氙 Xe
55 銫 Cs	56 鋇 Ba	鑭系	72 鉿 Hf	73 鉭 Ta	74 鎢 W	75 錸 Re	76 鋨 Os	77 銥 Ir	78 鉑 Pt	79 金 Au	80 汞 Hg	81 鉈 Tl	82 鉛 Pb	83 鉍 Bi	84 釙 Po	85 At	86 氡 Rn
87 Fr	88 鐳 Ra	錒系	104 * Rf	105 * Db	106 * Sg	107 * Bh	108 * Hs	109 * Mt	110	111							
鑭系元素		57 鑭 La	58 鈰 Ce	59 鐠 Pr	60 釹 Nd	61 Pm	62 釤 Sm	63 銪 Eu	64 釓 Gd	65 鋱 Tb	66 鏑 Dy	67 鈥 Ho	68 鉺 Er	69 銩 Tm	70 鐿 Yb	71 鎦 Lu	
錒系元素		89 錒 Ac	90 釷 Th	91 鏷 Pa	92 鈾 U	93 錼 Np	94 鈽 Pu	95 鋂 Am	96 鋦 Cm	97 Bk	98 Cf	99 鑀 Es	100 鐨 Fm	101 鍆 Md	102 No	103 鐒 Lr	

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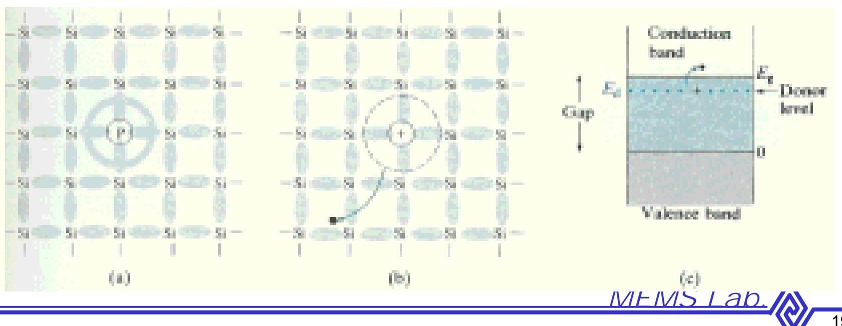
n-*Type Semiconductors*

- Silicon containing an Group V impurity such as phosphorus which has five valence electrons
- The extra electron of phosphorus can be pulled away with a small amount of energy



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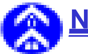
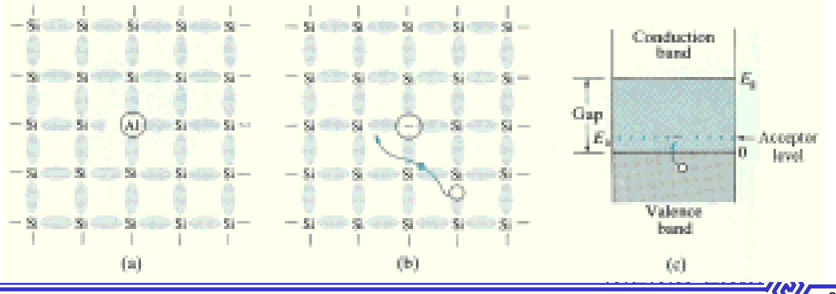


p-*Type Semiconductors*

- Silicon containing an Group III impurity such as aluminum (Al) and boron (B) which have only three valence electrons.
- This atom cancan accept an electron from the valence band, thus leaving the electron hole as a charge carrier.



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滲雜(Doping)的方式

- Diffusion
  - Furnace heating.
  - The doping atoms from the surrounding gas or a thin preapplied surface layer.
  - Main difficulty
    - Determination of the absolute concentration of the doping.
    - Only create a doping profile on the surface of a wafer.
- Ion implantation
  - Shooting charged doping ions, which are externally accelerated in a vacuum, into the silicon wafer.
  - The ions can penetrate up to a few micrometers below the surface.
  - The doping concentration gets an improved homogeneity, and the doping profile under the wafer's surface can be controlled more exactly.

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Comparison of Two Doping Methods

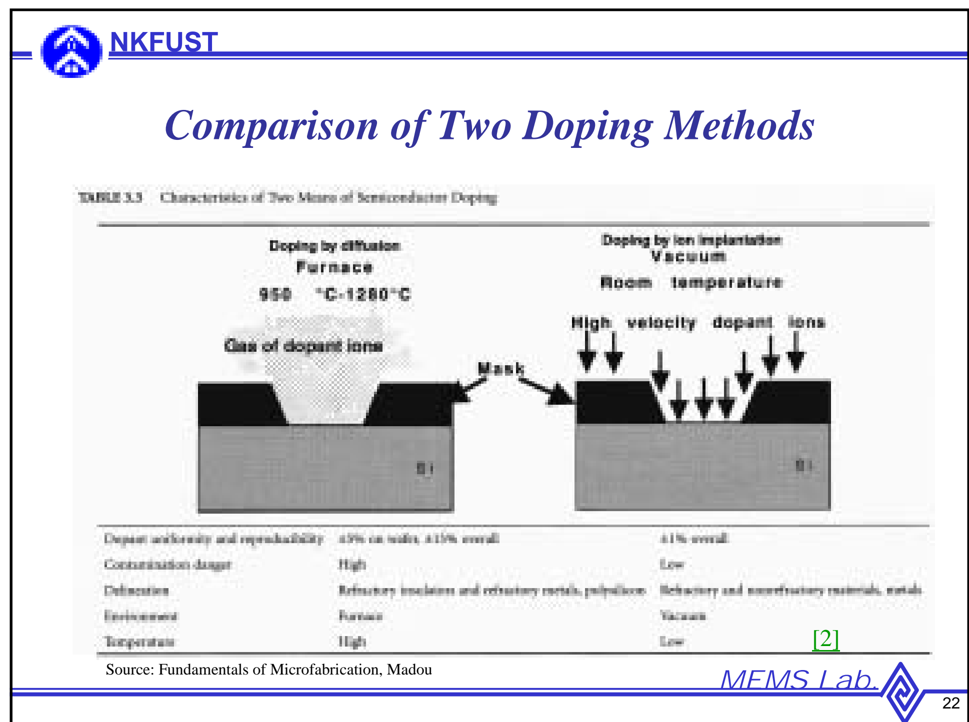

TABLE 3.3 Characteristics of Two Means of Semiconductor Doping

	Doping by diffusion	Doping by ion implantation
Dopant uniformity and reproducibility	±5% on wafer, ±15% overall	±1% overall
Contamination danger	High	Low
Delineation	Refractory insulators and refractory metals, polysilicon	Refractory and nonrefractory materials, metals
Environment	Furnace	Vacuum
Temperature	High	Low

[2]

Source: Fundamentals of Microfabrication, Madou

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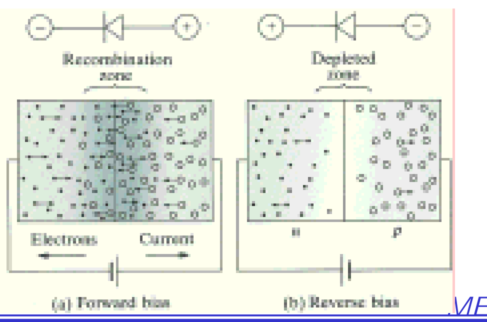
Semiconductor Devices - Diodes

- Junction Devices (Diodes)
  - Light-emitting diode (LED): When forward bias is added, carriers of both types cross the junction and recombine emitting a photon (GaAs produces red light).
  - The diode can also serve as a rectifier.



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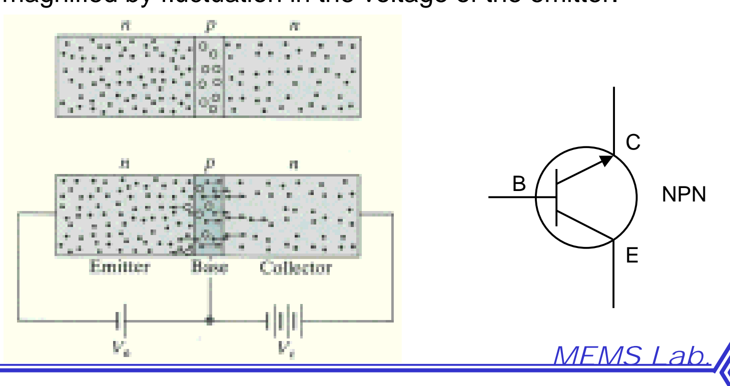
Semiconductor Devices - FET

- Field-Effect Transistors (FET)
  - Amplify weak signals to make strong, useable output.
  - n-p-n Transistor: The emitter to base current is highly magnified by fluctuation in the voltage of the emitter.



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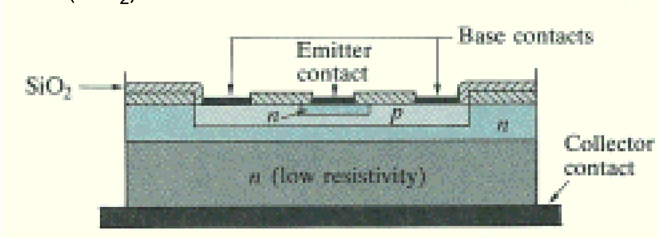
Semiconductor Processing

- Planar Transistor
  - Substrate: Low-resistivity, *n*-type, single crystal silicon.
  - Boron implanted into the surface of silicon to change the selected region into *p*-type.
  - A second masking and implantation step introduces a phosphorus to produce the *n*-type emitter.
  - Silica (SiO_2) as isolators. Aluminum as contact.



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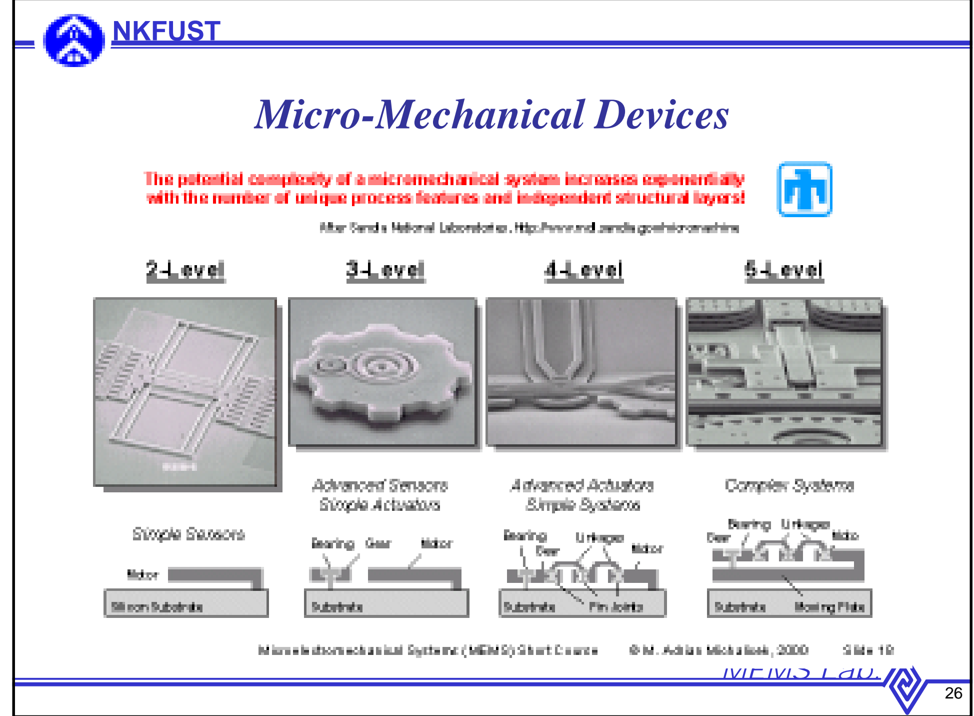
Micro-Mechanical Devices



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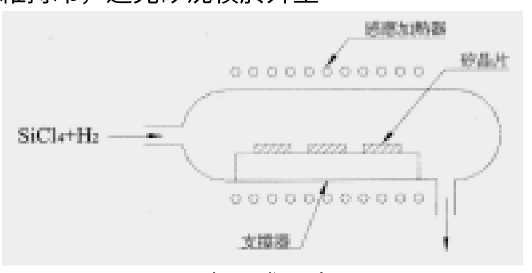
氣相磊晶

- 磊晶(Epitaxial)：以晶片的基板為成長的晶種，在低於熔點30~50%的溫度，以氣相(Vapor-Phase)持續累積單晶成長
  - $SiCl_4$（氣）+2H_2（氣）(>1000°C) →Si（固）+4HCl（氣）
  - 標準成長速率　1微米/分鐘
  - 外壁維持冷，避免矽沈積於外壁



[3]

水平式反應器

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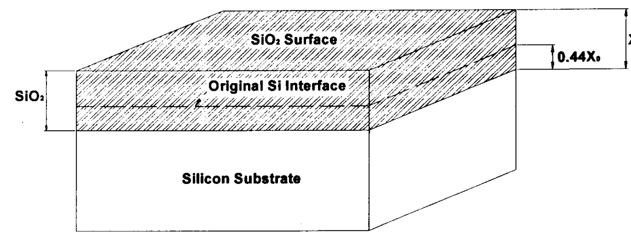
Thin Film Techniques

- Thermal Deposition of Silicon Oxide
  - Wet Oxidation
  - Dry Oxidation
- Physical Vapor Deposition (PVD)
  - Evaporation
  - Sputtering: DC-diode sputtering, Magnetron sputtering
- Chemical Vapor Deposition (CVD)
  - LPCVD, APCVD
  - Plasma Enhanced CVD (PECVD)
- Liquid Deposition
  - Galvanic, Spin coating, Catalytic

Thin Film Techniques - Thermal Deposition

- Thermal Deposition of Silicon Oxide
  - Native Oxide (oxidation in room temperature) 20Å
  - 高溫擴散能力快，氧化速度亦增加
  - 每產生厚度X_0的氧化層需消耗厚度X_S的矽晶片
    - $X_s = 0.44X_0$



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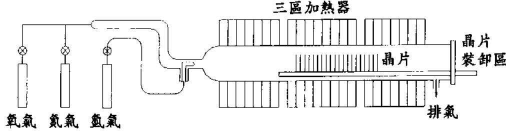
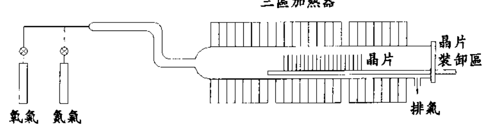
Thermal Oxidation

- Wet Oxidation: $Si_{(s)}+2H_2O_{(g)}\rightarrow SiO_{2(s)}+2H_{2(g)}$
  - 時間快



- Dry Oxidation: $Si_{(s)}+O_{2(g)}\rightarrow SiO_{2(s)}$
  - 熱爐管通入氧氣及適量氮氣或惰性氣體，慢慢加熱至900~1100°C（標準製程溫度）
  - 速度較慢但電性較佳，故在半導體產業中較常用



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Thin Film Techniques - PVD

- Physical Layer Deposition
  - 高硬度、耐腐蝕、美觀
  - Vapor Deposition
    - High temperature （接近熔點）in a vacuum chamber
    - Poor layer adhesion
  - Sputtering
    - Magnetron sputtering
    - Reactive sputtering
    - Better layer adhesion

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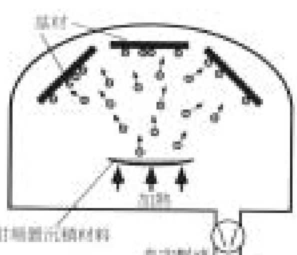
Physical Vapor Deposition (PVD)

- PVD依不同加熱源蒸鍍法可分為
  - 真空蒸鍍法、電子束蒸鍍法（常用）、雷射束蒸鍍法
- 真空蒸鍍法
  - Vacuum chamber
  - 電流通過坩堝加熱蒸鍍源至接近熔點
  - 蒸鍍源侷限於如鋁之低熔點金屬
  - 缺點：坩堝因被加熱，故可能造成沈積材料污染



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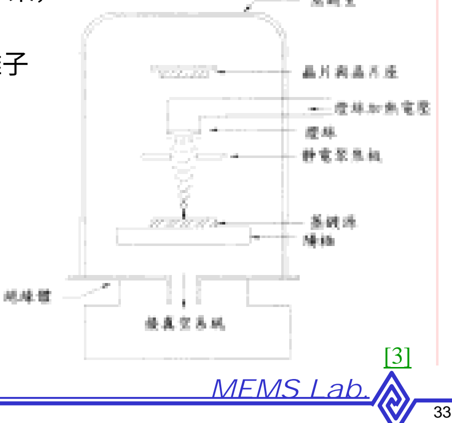
Physical Vapor Deposition (PVD)

- 電子束蒸鍍法 (Electron Beam Evaporation)
  - 因適用於高熔點材料，故較常用於半導體產業
  - 對燈絲加熱電壓使其產生電子束，經靜電聚焦板，加熱蒸鍍源。
  - 缺點：會產生X-Ray或其他離子而破壞基材
- 雷射束蒸鍍法
  - 以雷射束取代電子束
  - 不會破壞基材，但昂貴



[3]

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Physical Vapor Deposition (PVD)

- 限制與缺點
  - 沈積率低
  - 不同材料熔點與蒸發速率不同，因此對合金或化合物得沈積成分控制不易
  - 薄膜對階梯的覆蓋能力差
  - 加熱源易對薄膜品質造成污染
- 一般精密的半導體製程與VLSI多以濺鍍法取代蒸鍍法

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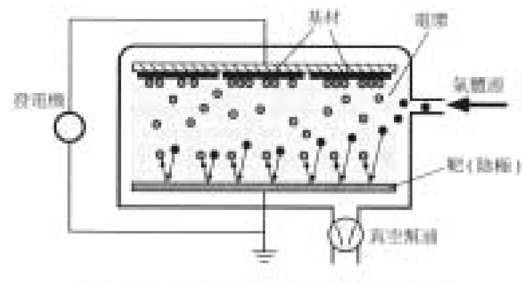
濺鍍 (Sputtering)

- 基本原理（直流濺鍍）
  - 氣體輝光放電廠生電漿
  - 帶電正離子經電場加速撞擊靶材
  - 靶材被轟擊出原子與離子，原子藉由動能及擴散原理在晶片表面進行沈積



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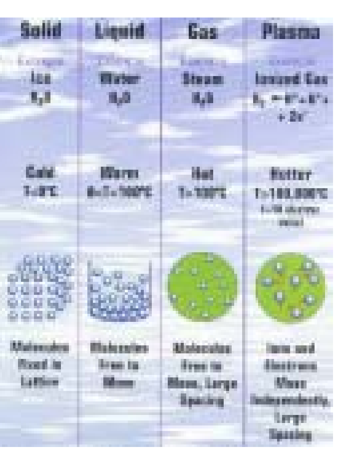
What's Plasmas

- The Fourth State of Matter
  - Freely moving charged gas particles, i.e., electrons and ions.（離子化的氣體）
  - Formed at high temperatures.
  - Can be accelerated and steered by electric and magnetic fields.



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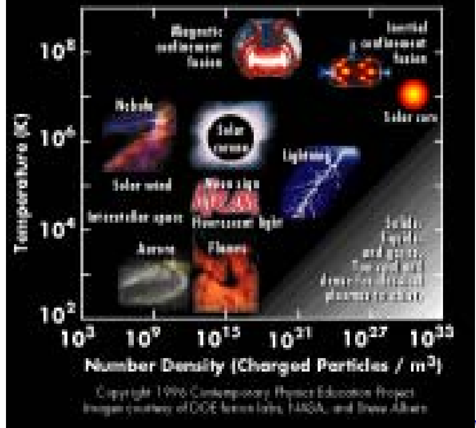
Types of Plasma

- Plasma in various densities and temperatures



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濺鍍種類

- 直流濺鍍 (DC-diode Sputtering)
  - 靶材接陰電極，基材接陽極
  - 沈積率不高
- 磁控濺鍍(Magnetron Sputtering)
  - 靶材背面加上磁場
  - 電磁作用會產生二次電子
    增加電漿濃度，因而增加沈積率
  - 減少氣體離子對基材與容器壁漫
    無方向的碰撞
  - 因電離率增加，可減少氣體消耗
- 非平衡磁控濺鍍（UBM）

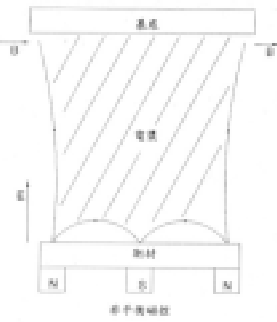

圖 2.4.11 非平衡磁控濺鍍法的磁力線範圍(E：電場方向 B：磁場方向) [3]

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濺鍍種類

- 高週波濺鍍(Radio-Frequency Sputtering)
  - 若靶材為非導體時，氣體離子撞擊靶材後得不到電子中和，使正電荷累積，與後來的氣體離子排斥
  - 以高週波取代直流電
  - 正離子撞擊靶材（陰極）後，將陰陽極調換，陰陽變換，此時電子撞擊變成陽極的靶材，以中和其上的正電荷
- 反應性氣體濺鍍(Reactive Gas Sputtering)
  - 將少許反應性氣體如N2, O2，烷類等，隨同惰性氣體輸入真空腔，使反應氣體與靶材原子一起沈積於基底，以改變薄膜成分
- 封閉式非平衡磁控濺鍍法

蒸鍍法與濺鍍法的比較

	蒸鍍法	濺鍍法
靶材的選擇	受限制（金屬靶材）	幾乎不受限
基材加熱	低	除磁控法外，需高溫
表面損害	低，電子束會產生 X-ray 損害	離子轟擊的損害
合金沈積	否	可
均勻度	難	易
厚度控制	不易控制	易控制
沈積種類	一次只能沈積一種薄膜	可以沈積多層膜
附著性	不佳	佳
薄膜性質	不易控制	可利用調偏壓、壓力、基材加熱來控制
基本設備費	低價格	昂貴

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Thin Film Techniques - CVD

- Chemical Layer Deposition
  - Predominantly used in thin film technology
  - Exactly dosed, good thickness control and physical property
  - Extremely high purity
  - Applicable materials: Silicon Oxide (SiO_2), Silicon Nitride(Si_3N_4), Polycrystalline Silicon, Epitaxy
  - Disadvantages: High process temperature (~1250°C) and toxic gases

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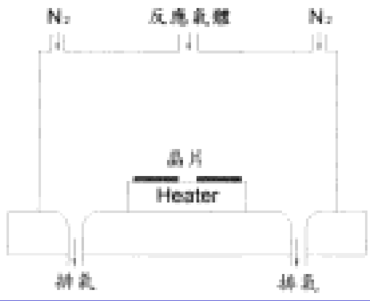
Various type of CVD

- Atmospheric Pressure Chemical Vapor Deposition (APCVD)
  - 通常用來沈積磊晶矽及複合半導體材料
  - 在300　450ºC低溫下通過反應氣體，可高速沈積二氧化矽
  - 冷壁式以減少壁面沈積
  - 階梯覆蓋性較差



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Various type of CVD

- Low Pressure Chemical Vapor Deposition (LPCVD)
  - 壓力在10Pa以下
  - 通常用來沈積多晶矽
  - 階梯覆蓋性較佳，但沈積速率較慢
  - 熱管壁設計，故需定期清理管壁

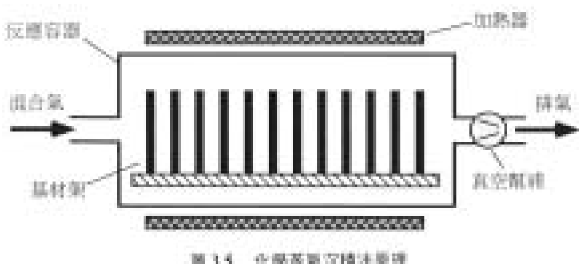

圖 3.5 化學蒸氣沉積法原理

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Various type of CVD

- Plasma Enhanced CVD (PECVD)
  - 150~350 °C
  - High energy electrons break the chemical bonds and ionize the molecules of the layer material.
  - Better deposition rate and uniformity
- Metal Organic CVD (MOCVD)
  - 將氫化物（如砷化三氫）或有機金屬聚合物（三聚乙基鎵）的反應氣體，於流場通過試片置放處進行薄膜沉積

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CVD薄膜材料與沈積方式

- CVD常用材料
  - 二氧化矽(SiO_2)：蝕刻阻擋層、防護層、閘氧化層、隔離層
  - 磷矽玻璃(PSG)：犧牲層
  - 多晶矽(Polycrystalline Silicon)：作為結構層
  - 氮化矽(Si_3N_4): 蝕刻保護層
  - 碳化矽(Silicon Carbide):作為結構層
  - 鎢(W)：導體

表 2.4.3 CVD 薄膜材料與沈積方式的關係

不同 CVD 的方法	薄膜材料
LP	SiO_2、Si_3N_4、Polysilicon 、WSi_x、 W
AP	SiO_2、PSG、BPSG
PE	SiO_2、PSG、BPSG、Si_3N_4、SiO_xN_y

Polysilicon

- LPCVD: source gas SiH_4, 570-650°C, 100~400 mtorr, 100 Å/min (630 °C)
- Microstructure depends on deposition condition
  - 100% SiH_4 source gas, 100 mtorr, temp < 570°C, produces amorphous film
  - 100% SiH_4 source gas, 100 mtorr, temp > 570°C, produces polycrystalline film
    - 600 °C, grains are fine and equiaxed
    - 625 °C, grains are large and have a columnar structure
    - Crystalline orientation of the polysilicon grain is predominantly (110) for substrate temp. 600~650°C, and is predominantly (100) for substrate temp. 650~700°C

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Silicon Dioxide

- Masking（阻擋層）
  - Diffusion Masking（擴散阻擋層）
  - Ion Implantation Masking（離子植入阻擋層）
  - Etching Masking（蝕刻阻擋層）
- Passivation（防護層）：保護晶片表面以減少離子植入時的破壞
- Gate Oxide（閘氧化層）：MOS閘氧化層及電容的介電層
- Isolation（隔離層）：元件與元件隔離之場氧化層
- Sacrificial Layer（犧牲層）：搭配多晶矽作為懸浮結構的犧牲層

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SiO_2氧化層的製作 - 1

- 熱氧化(Thermal Oxidation)
  - Self-limiting process to about 2 μm
  - Structure more dense than LPCVD SiO_2
  - Compressive residue stress
- LPCVD
  - Also called Low-temperature oxidation (LTO)
  - Use SiH_4 and O_2 as precursor gases at temperature of 425 to 450 °C and pressure of 200~400 mtorr
  - Could produce thick film (> 2 μm), typically 100 Å/min
  - Include dopant gases, such as PH_3, to make phosphosilicate glass (PSG)
  - Tensile residue stress (PSG < LTO)

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SiO_2氧化層的製作 - 2

- PECVD
  - Low-stress and very thick film (10 to 20 μm), using thin Si_3N_4 in conjuction with the thick SiO_2 film to create crack-free SiO_2 film.
  - Use tetraethylorthosilicate (TEOS) as precursor gases
- Crystalline SiO_2 (quartz)
  - Piezoelectric
  - Electrically insulating
- Spin-on-Glass (SOG)
  - Spin-coating to produce thick (20 μm) film in conjunction with CMP
  - Used as a thick film sacrificial molding material to pattern thick polysilicon
- Etch rate in HF: PSG > LTO > thermal oxide

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Silicon Nitride

- PECVD
  - $SiH_4 + NH_3$ (or N_2) – (200~400°C, RF)→ $Si_xN_yH_z + H_2$
  - Nearly stress-free but high etch rate in HF due to porosity structure
  - 沈積速度約5分鐘0.1微米厚
- LPCVD
  - $3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$, $NH_3 : SiCl_2H_2 = 10:1$
  - 700~900°C, 200~500 mtorr, 沈積速度約 20分鐘0.1微米厚
  - Stochiometric and amorphous structure, resistant to chemical
  - Thick film tends to crack due to large tensile residue stress
- Low-stress Nitride: "Silicon-rich"
  - LPCVD 850°C, 500 mtorr, $NH_3 : SiCl_2H_2 = 1:6$
  - Nonstochiometric Si_xN_y, Lower etch rate in HF

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二氧化矽與氮化矽薄膜的顏色

- 熱成長的二氧化矽（折射率1.48）與氮化矽（折射率1.97）的顏色表

顏色	二氧化矽之厚度 (Å)	氮化矽之厚度 (Å)
銀色	< 270	< 200
棕色	< 530	< 400
黃—棕色	< 730	< 550
紅色	< 970	< 730
深藍色	< 1000	< 770
藍色	< 1200	< 930
淡藍色	< 1300	< 1000
極淡藍色	< 1500	< 1100
綠色	< 1600	< 1200
淡黃色	< 1700	< 1300
黃色	< 2000	< 1500
橘紅色	< 2400	< 1800
紅色	< 2500	< 1900
深紅色	< 2800	< 2100
藍色	< 3100	< 2300
藍綠色	< 3300	< 2500
淡綠色	< 3700	< 2800
橘黃色	< 4000	< 3000
紅色	< 4400	< 3300

[4]

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Silicon Carbide

- Polymorphic material: multicrystalline structures (cubic, hexagonal, and rhombehedral), each sharing a common stoichiometry
- Use APCVD or LPCVD
- Extremely hard and strong, doesn't melt.
- Can be etched in KOH but 600°C
- Thin film can be dry etched with RIE
  - Using CHF_3 or SF_6 combined with O_2
  - Must use metal, such as AL and Ni, as masking material (since high O_2 content will attack PR)

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常見CVD的比較

表 2.4.4 常見 CVD 沈積方式的比較

沈積方式	優點	缺點	壓力.溫度
APCVD	構造簡單、高沈積率、低溫	階梯覆蓋差、微粒污染	10~100kPa 350~400℃
LPCVD	薄膜純度佳且均勻、階梯覆蓋適當	高溫、低沈積率	100Pa 550~600℃
PECVD	溫度低、附著性好及階梯覆蓋佳、針孔密度低	微粒污染	2-5Torr ~300~400℃
MOCVD	對大面積有極佳的取向附生	安全考量	

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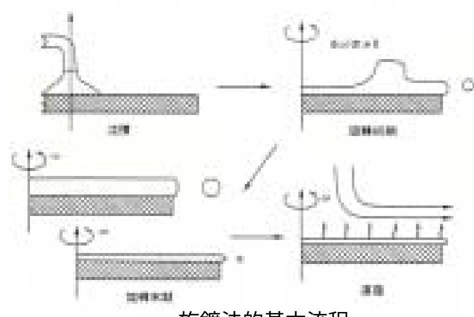
Thin Film Techniques – Liquid Phase

- Liquid phase deposition : galvanic, spin-coating, catalytic
  - Galvanic（電鍍）
  - Spin Coating（旋鍍法）：一般用於光阻(photoresisit)塗佈
  - Catalytic method （電解法）：僅適用於金屬



旋鍍法的基本流程

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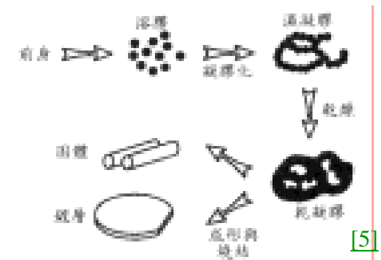
溶膠—凝膠沈積法

- 溶膠—凝膠沈積法(Sol-gel)
  - 將薄膜中的相關材料成分混合於溶劑中形成溶膠狀的precursor
  - 以Spin coating塗佈presursor形成均勻薄膜，溶膠狀懸浮中的固體粒子經化學反應構成凝膠狀的網絡
  - 熱處理後，移除溶劑可將凝膠網絡轉換成固相
  - 常用材料：二氧化矽、氮化矽、氧化鋁、鋯鈦酸鉛(PZT)



[5]

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Piezoresistivity

- 壓阻性Piezoresistance: 材料電阻值會受材料應變所改變
- 大部分材料都具有壓阻特性
- 半導體材料如Si與Ge其壓阻係數比金屬大一個order
  - σ_l, σ_t: Longitudinal （與電流方向平行）and transverse （與電流方向垂直） stress component
  - π_l, π_t: Longitudinal and transverse piezoresistance coefficient

$$\frac{\Delta R}{R} = \sigma_l \pi_l + \sigma_t \pi_t$$

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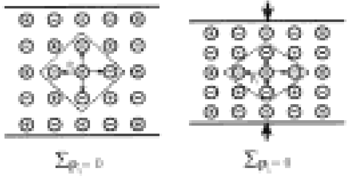
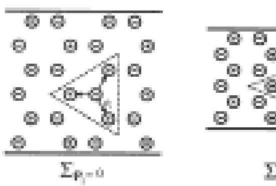
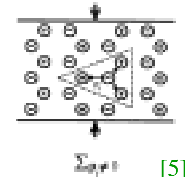
Piezoelectric Material

- 壓電(Piezoelectric)現象是一種存在某些材料的機電轉換
  - 1880由居禮兩兄弟在石英發現的特性
  - 無外加電場：正電與負電荷的中心不重合產生淨電雙極，整個晶體因而產生淨極化(polarization)
  - 在材料的居禮溫度以上經體會便成立方晶，因而失去壓電性







[5]

圖 2.5。在一個假想的二維晶格之中，消失的雙極的說明，一個擁有對稱中心的晶體不可能是壓電性的，這是因為基本單元之內雙極一定會彼此抵銷掉，因此，在晶體之內不會有淨極化，一個外加的應力並不會改變對稱中心。引用 Middelhoek 與 Audet [12]。

圖 2.6 在一個二維晶體之中的壓電性的說明，當外加一個應力時，一個欠缺對稱中心的離子晶體的基本單元之內的淨電雙極並不會消失，這是壓電性的物理起源，引用 Middelhoek 與 Audet [12]。

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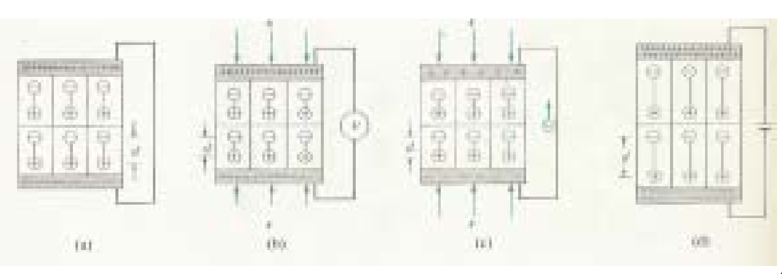
Piezoelectric Material

- 主要的壓電材料：Quartz(SiO_2 crystal), PZT, PVDF, ZnO, $LiNbO_3$, $BaTiO_3$
- 正壓電效應：外加壓力產生電位差
- 逆壓電效應：外加電場使壓電材料產生變形



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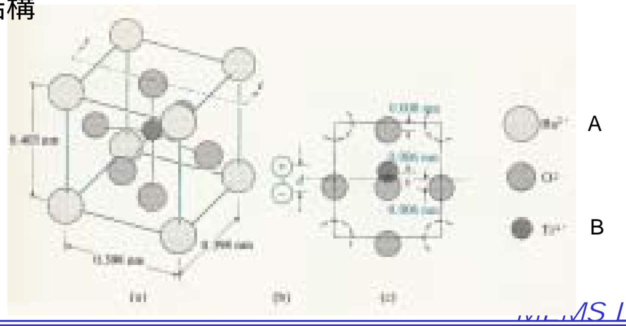
鐵電(Ferroelectric)材料的晶格結構

- 鈣鈦礦結構是鐵電材料中最常見的一種，化學式為ABO_3
- Electric Dipole: 正、負電荷的中心不重合，具有自發極化
- $BaTiO_3$、PZT（鈦酸鉛和鋯酸鉛）、$LiNbO_3$等化合物為鈣鈦礦結構



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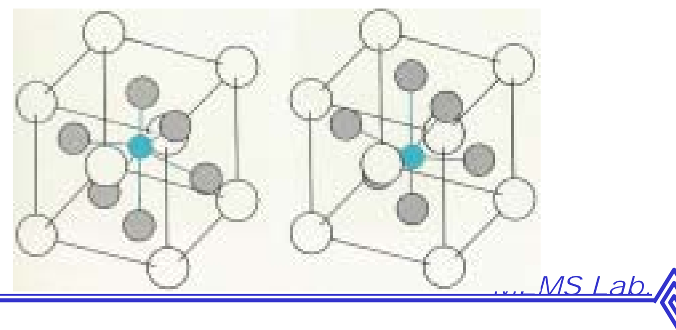
Ferroelectricity

- 所有鐵電(Ferroelectric)材料具有壓電(Piezoelectricity)效應
- 材料本身極化方向可藉由外加電場加以改變，稱為鐵電效應(Ferroelectricity)
- 外加電場可改變$BaTiO_3$極化方向的



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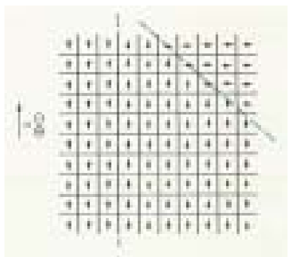
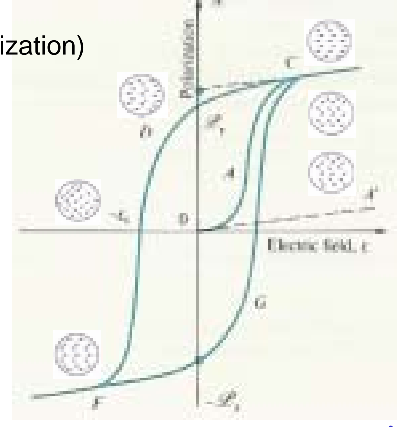
Ferroelectric Hysteresis

- PE Diagram
  - Hysteresis loop: CDFGC
  - Pr:殘留極化(Remanent polarization)
  - $-\varepsilon_c$: 矯頑電場(Coercive field)
  - Ferroelectric Domains





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